

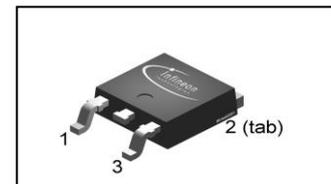
OptiMOS[®]-T Power-Transistor

Features

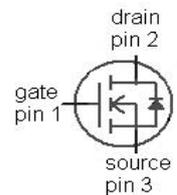
- N-channel - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	24	mΩ
I_D	35	A

PG-TO252-3-11


Type	Package	Marking
IPD35N10S3L-26	PG-TO252-3-11	3N10L26


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{°C}, V_{GS}=10\text{V}$	35	A
		$T_C=100\text{°C}, V_{GS}=10\text{V}^{1)}$	25	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{°C}$	140	
Avalanche energy, single pulse ¹⁾	E_{AS}	$I_D=17\text{A}$	175	mJ
Avalanche current, single pulse	I_{AS}		35	A
Gate source voltage ²⁾	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{°C}$	71	W
Operating and storage temperature	T_j, T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics¹⁾

Thermal resistance, junction - case	R_{thJC}		-	-	2.1	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS}=0V, I_D=1\text{mA}$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=39\mu\text{A}$	1.2	1.7	2.4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	0.01	0.1	μA
		$V_{DS}=80V, V_{GS}=0V, T_j=125^\circ\text{C}^{1)}$	-	1	10	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=35A$	-	24.5	31.9	m Ω
		$V_{GS}=10V, I_D=35A$	-	20.0	24.0	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics¹⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	2070	2700	pF
Output capacitance	C_{oss}		-	460	600	
Reverse transfer capacitance	C_{rss}		-	50	75	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=35A, R_G=3.5\Omega$	-	6	-	ns
Rise time	t_r		-	4	-	
Turn-off delay time	$t_{d(off)}$		-	18	-	
Fall time	t_f		-	3	-	

Gate Charge Characteristics¹⁾

Gate to source charge	Q_{gs}	$V_{DD}=80V, I_D=35A,$ $V_{GS}=0$ to 10V	-	8	10	nC
Gate to drain charge	Q_{gd}		-	5	8	
Gate charge total	Q_g		-	30	39	
Gate plateau voltage	$V_{plateau}$		-	3.7	-	V

Reverse Diode

Diode continuous forward current ¹⁾	I_S	$T_C=25^\circ C$	-	-	35	A
Diode pulse current ¹⁾	$I_{S,pulse}$		-	-	140	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=35A,$ $T_j=25^\circ C$	0.6	1	1.2	V
Reverse recovery time ¹⁾	t_{rr}	$V_R=50V, I_F=I_S,$ $di_F/dt=100A/\mu s$	-	79	-	ns
Reverse recovery charge ¹⁾	Q_{rr}		-	150	-	

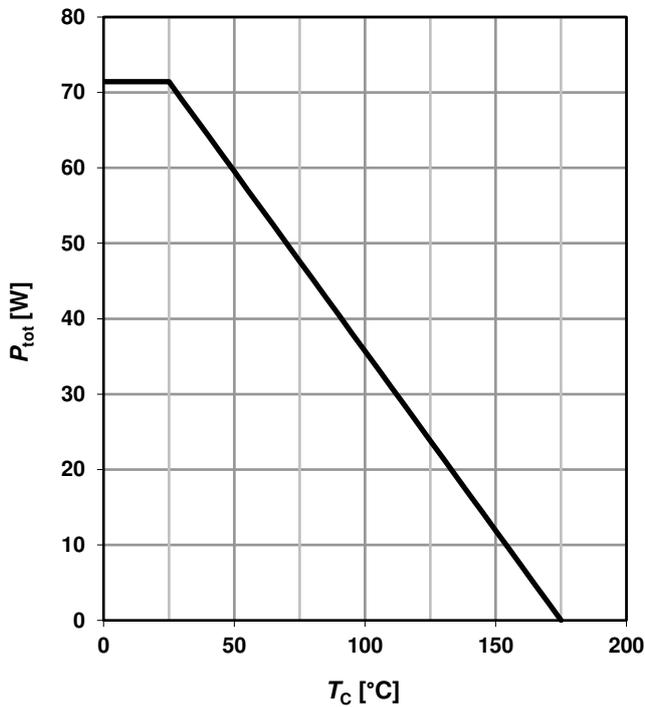
¹⁾ Defined by design. Not subject to production test.

²⁾ -5V to -20V for max. 168 non-consecutive hours.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

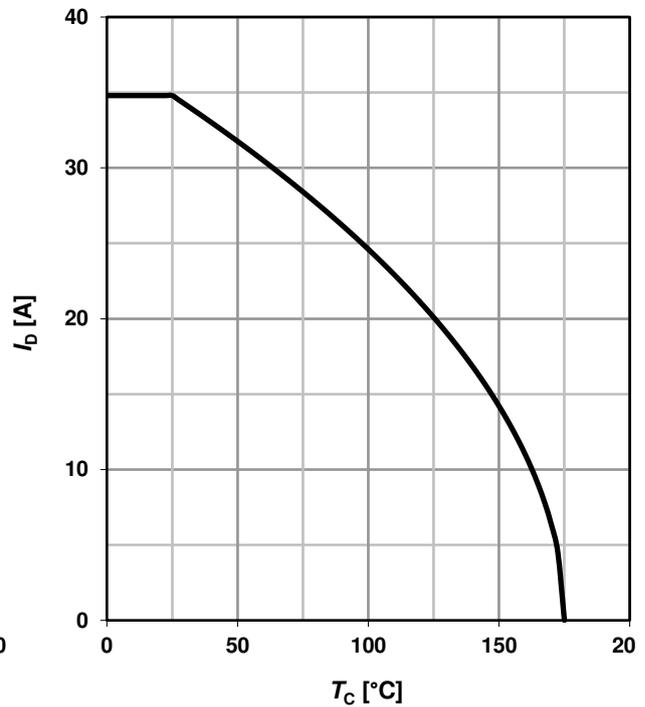
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6\text{ V}$



2 Drain current

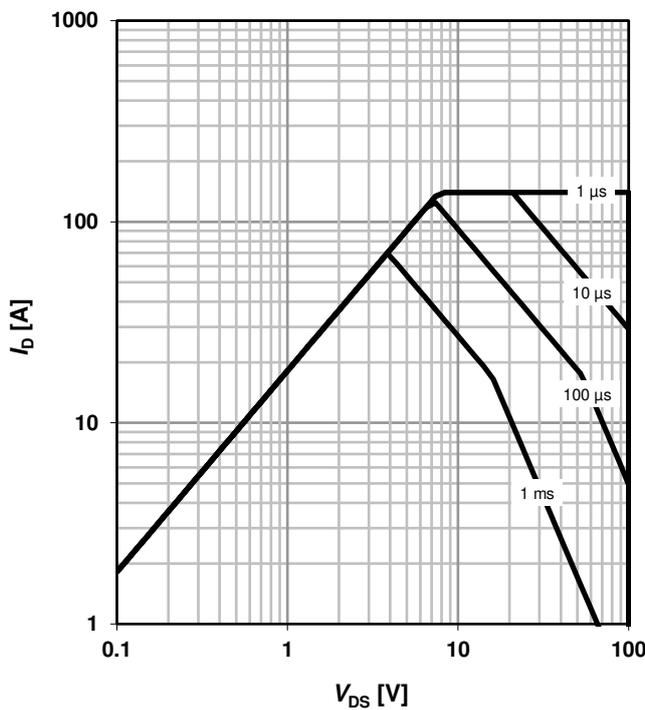
$I_D = f(T_C); V_{GS} \geq 6\text{ V}$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

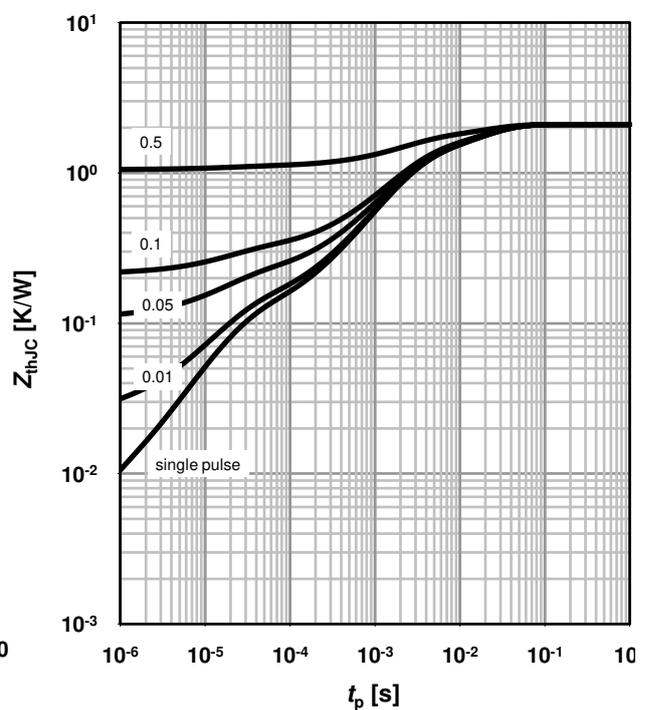
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

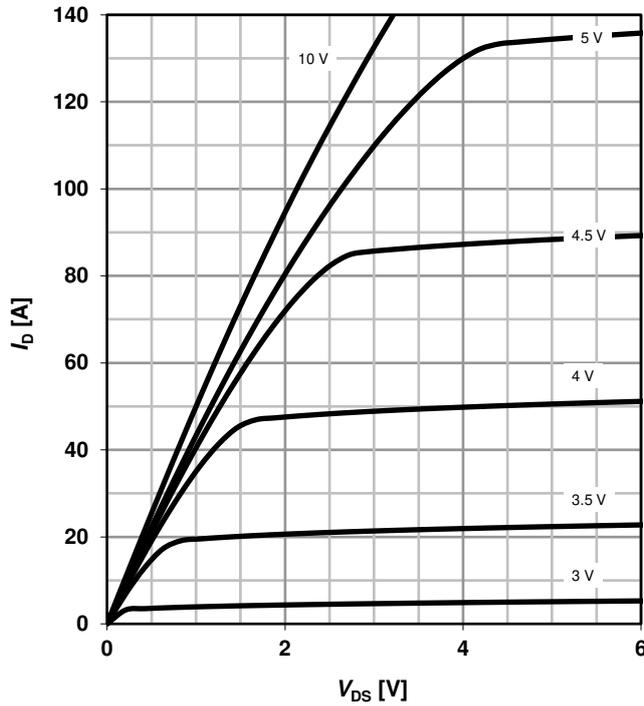
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

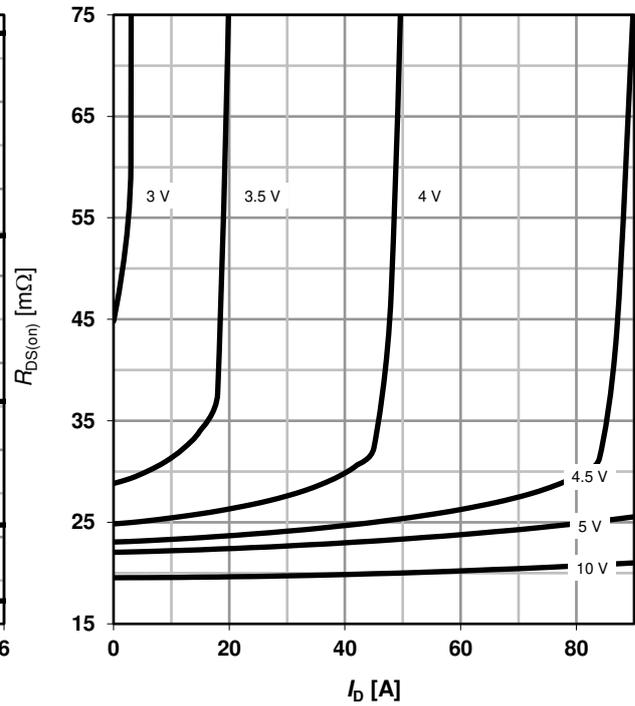
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

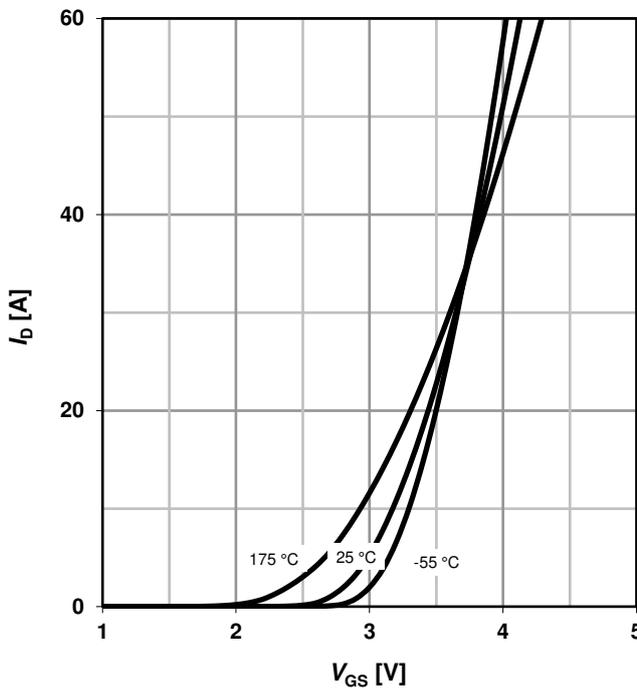
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

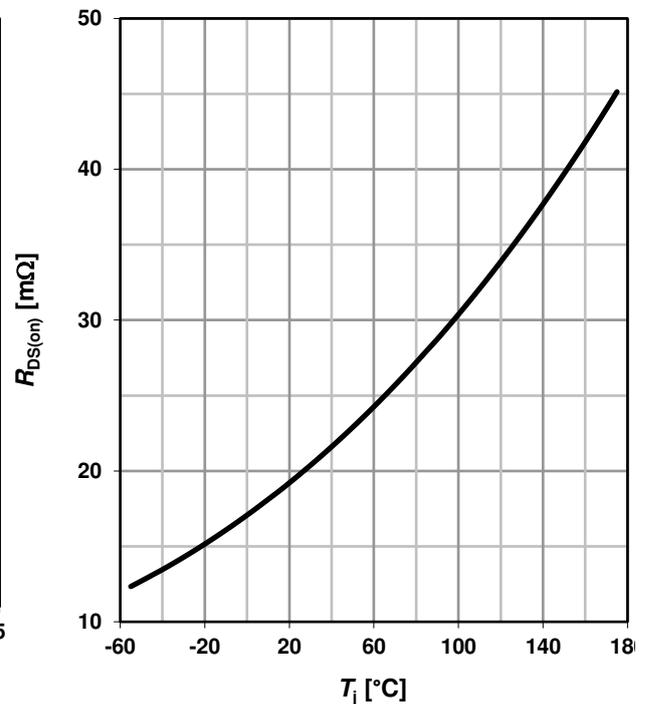
parameter: T_j



8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j); I_D = 30\text{ A}; V_{GS} = 10\text{ V}$

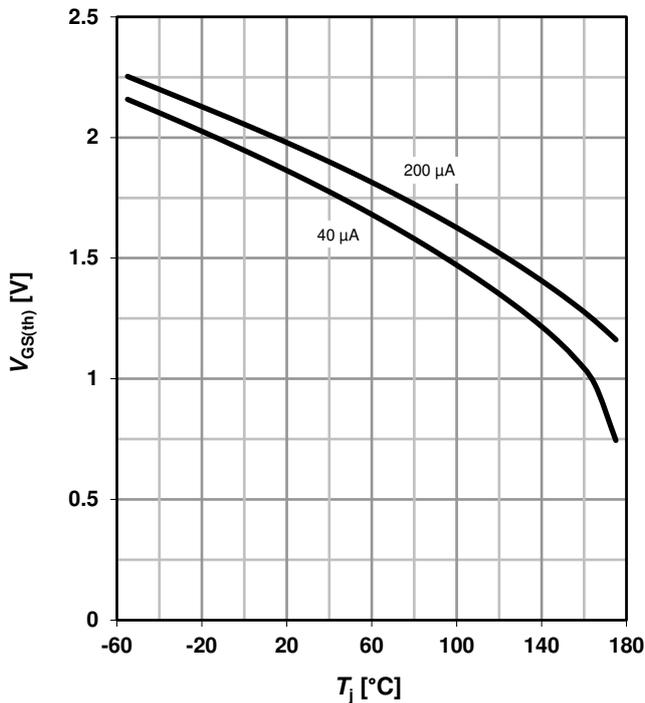
$\alpha = 0.56$



9 Typ. gate threshold voltage

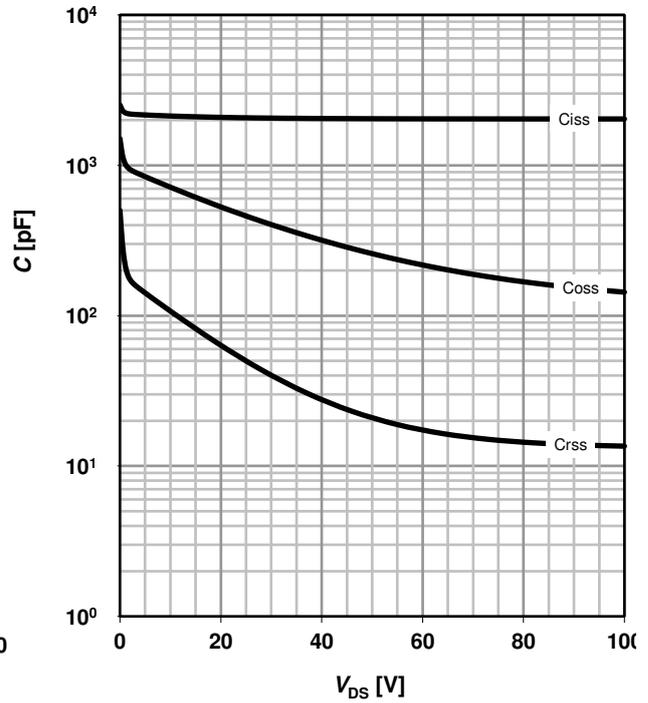
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

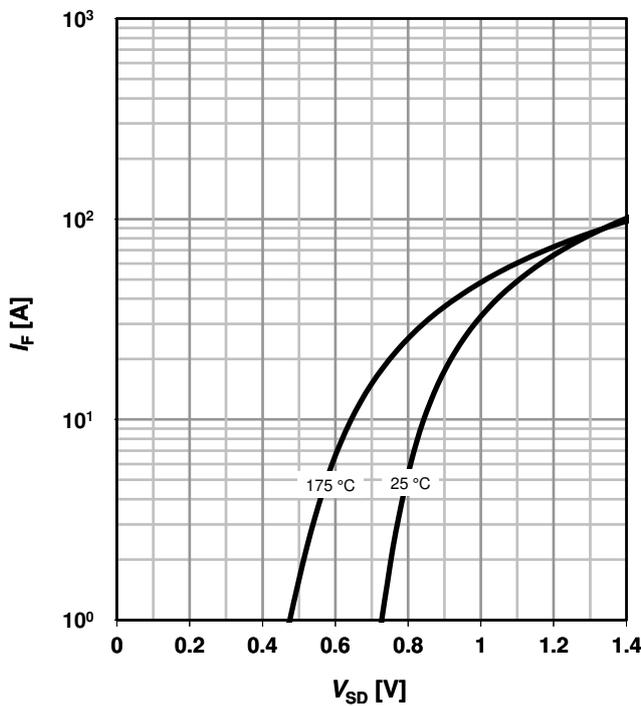
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

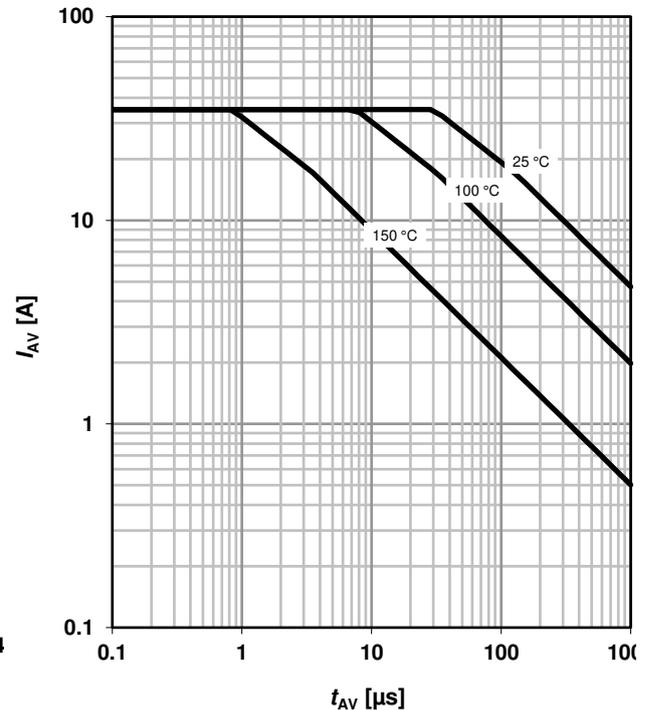
parameter: T_j



12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

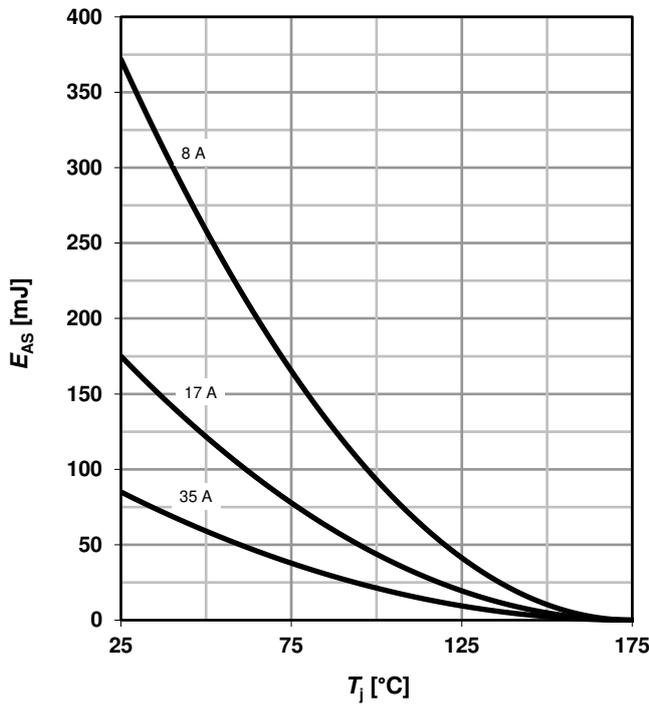
parameter: $T_{j(start)}$



13 Typical avalanche energy

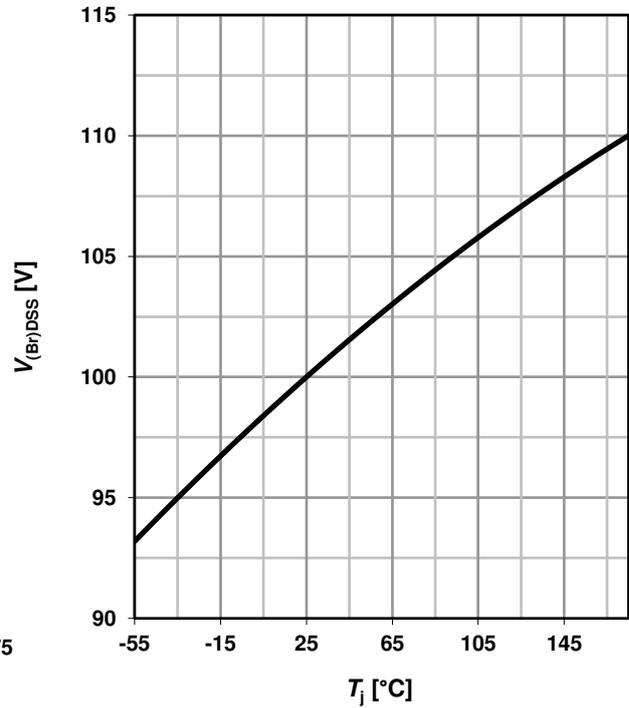
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Typ. drain-source breakdown voltage

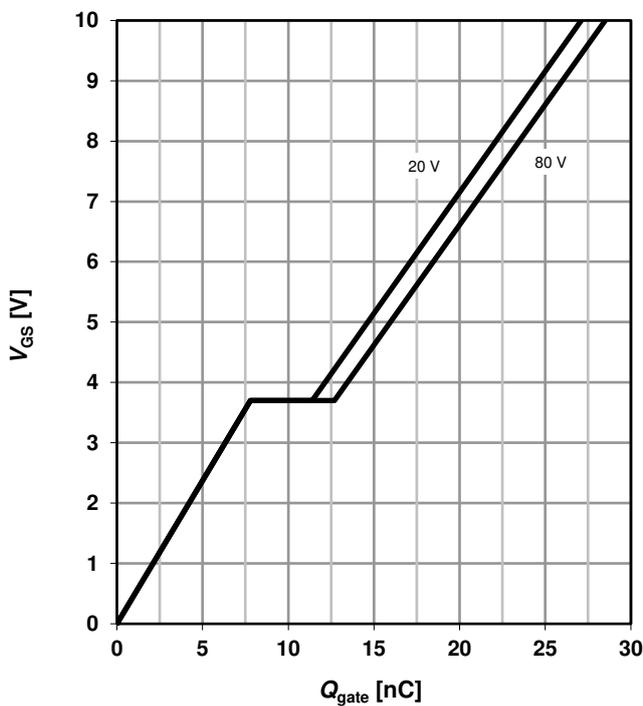
$$V_{(Br)DSS} = f(T_j); I_D = 1 \text{ mA}$$



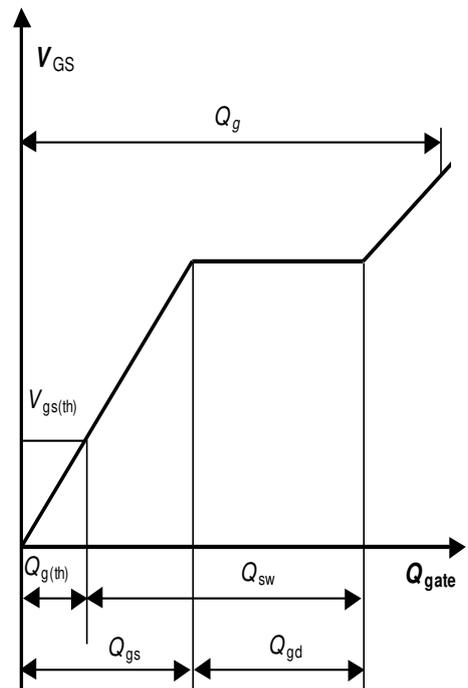
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 35 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Edition 2023-06-15**Published by****Infineon Technologies AG****81726 Munich, Germany****© 2023 Infineon Technologies AG****All Rights Reserved.****Do you have any questions about any aspect of this document?****Email: erratum@infineon.com****Document reference****IPD35N10S3L-26-Data-Sheet-13-Infineon****IMPORTANT NOTICE**

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Revision History

Version	Date	Changes
Rev 1.0	21.04.2008	Final data sheet
Rev 1.1	17.05.2011	$I_{D,pulse}$ corrected
Rev 1.2	15.06.2023	$R_{DS(on),max}$ in Product Summary corrected
Rev 1.2	15.06.2023	Diagram 8 Typ. drain-source on-state resistance: used α value clarified
Rev 1.2	15.06.2023	Ratings of Gate Source Voltage V_{GS} refined in footnote ²⁾
Rev 1.2	15.06.2023	Corrected diagram 3 safe operating area
Rev 1.2	15.06.2023	Corrected diagram 10 typical capacitances