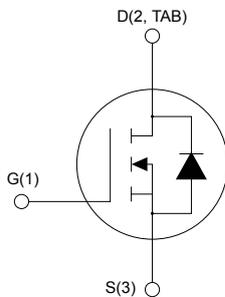
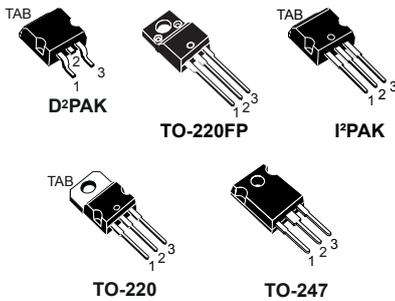




STB11NM80T4, STF11NM80, STI11NM80 STP11NM80, STW11NM80

Datasheet

N-channel 800 V, 380 mΩ typ., 11 A MDmesh Power MOSFETs
in D²PAK, TO-220FP, I²PAK, TO-220 and TO-247 packages



AM01475v1_noZen



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STB11NM80T4	800 V	400 mΩ	11 A
STF11NM80			
STI11NM80			
STP11NM80			
STW11NM80			

- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance
- 100% avalanche tested

Applications

- Switching applications

Description

These N-channel Power MOSFETs are developed using STMicroelectronics' revolutionary MDmesh technology, which associates the multiple drain process with the company's PowerMESH horizontal layout. These devices offer extremely low on-resistance, high dv/dt and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, these Power MOSFETs boast an overall dynamic performance which is superior to similar products on the market.

Product status links

[STB11NM80T4](#)
[STF11NM80](#)
[STI11NM80](#)
[STP11NM80](#)
[STW11NM80](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, I ² PAK, TO-220 TO-247	TO-220FP	
V _{DS}	Drain-source voltage	800		V
V _{GS}	Gate-source voltage	±30		V
I _D	Drain current (continuous) at T _C = 25 °C	11	11 ⁽¹⁾	A
	Drain current (continuous) at T _C = 100 °C	8	8 ⁽¹⁾	
I _{DM} ⁽²⁾	Drain current (pulsed)	44	44 ⁽¹⁾	A
P _{TOT}	Total power dissipation at T _C = 25 °C	150	35	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	30		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T _C = 25 °C)	2.5		kV
T _{stg}	Storage temperature range	-65 to 150		°C
T _J	Operation junction temperature range			°C

- Limited by maximum junction temperature.
- Pulse width is limited by safe operating area.
- V_{DD} = 640 V, I_{SD} = 11 A.

Table 2. Thermal data

Symbol	Parameter	Value					Unit
		D ² PAK	TO-220FP	I ² PAK	TO-220	TO-247	
R _{thJC}	Thermal resistance, junction-to-case	0.83	3.6	0.83		°C/W	
R _{thJA}	Thermal resistance, junction-to-ambient	30 ⁽¹⁾	62.5		50	°C/W	

- When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _J max.)	2.5	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	400	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\ \text{V}$, $V_{DS} = 800\ \text{V}$			10	μA
		$V_{GS} = 0\ \text{V}$, $V_{DS} = 800\ \text{V}$, $T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate body leakage current	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 30\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}$, $I_D = 5.5\ \text{A}$		380	400	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0\ \text{V}$	-	1630	-	pF
C_{oss}	Output capacitance		-	750	-	pF
C_{rSS}	Reverse transfer capacitance		-	30	-	pF
Q_g	Total gate charge	$V_{DD} = 640\ \text{V}$, $I_D = 11\ \text{A}$, $V_{GS} = 0\ \text{to}\ 10\ \text{V}$ (see the Figure 16. Test circuit for gate charge behavior)	-	50	-	nC
Q_{gs}	Gate-source charge		-	12	-	nC
Q_{gd}	Gate-drain charge		-	21	-	nC
R_g	Gate input resistance	$f = 1\ \text{MHz}$, open drain	-	2.7	-	Ω

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\ \text{V}$, $I_D = 5.5\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\ \text{V}$	-	22	-	ns
t_r	Rise time		-	17	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	46	-	ns
t_f	Fall time		-	15	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.86		V
t_{rr}	Reverse recovery time	$I_{SD} = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	612		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 50\text{ V}$	-	7.22		μC
I_{RRM}	Reverse recovery current	(see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	23.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	970		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 50\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	11.25		μC
I_{RRM}	Reverse recovery current	(see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	23.2		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

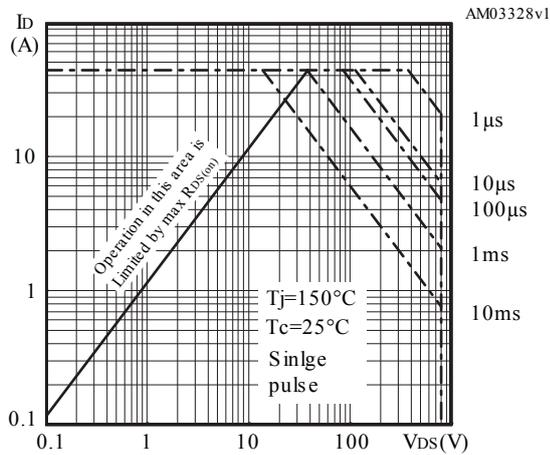
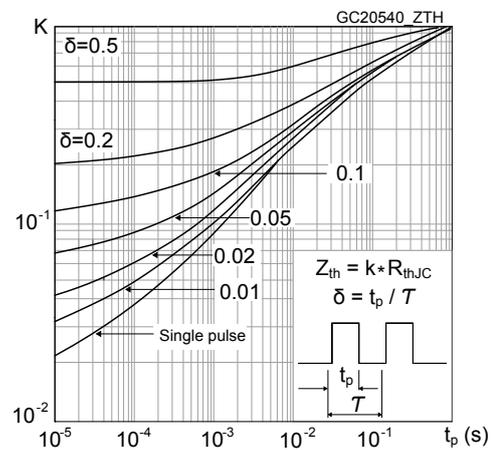
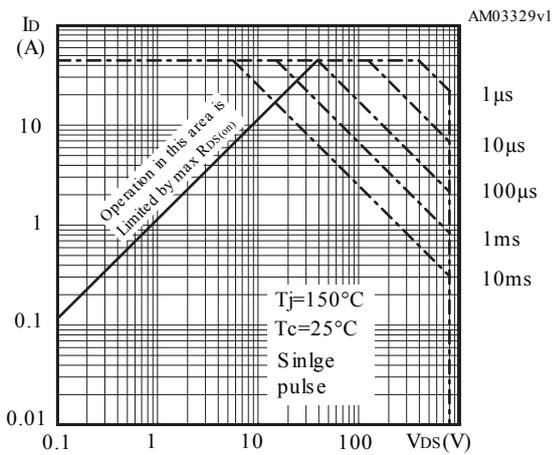
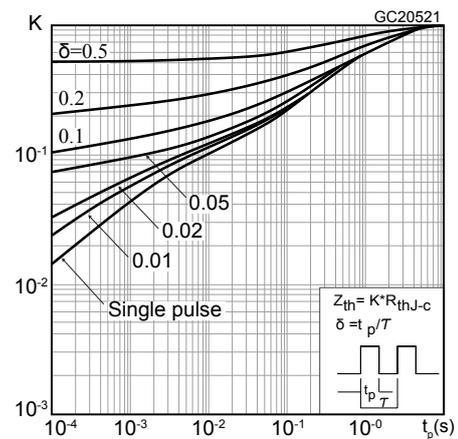
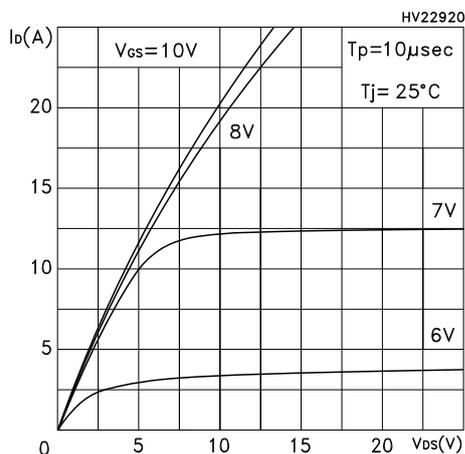
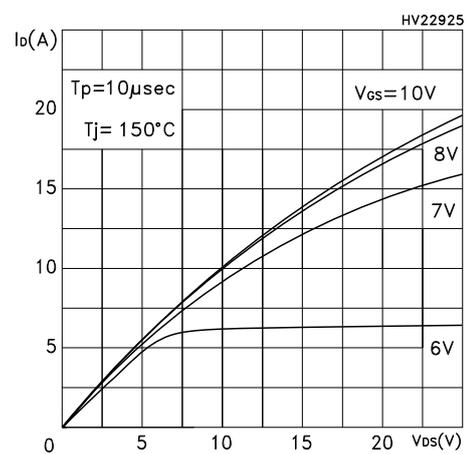
2.1 Electrical characteristics (curves)
Figure 1. Safe operating area for D²PAK, I²PAK, TO-220 and TO-247

Figure 2. Normalized transient thermal impedance for D²PAK, I²PAK, TO-220 and TO-247

Figure 3. Safe operating area for TO-220FP

Figure 4. Normalized transient thermal impedance for TO-220FP

Figure 5. Typical output characteristics at T_j = 25 °C

Figure 6. Typical output characteristics at T_j = 150 °C


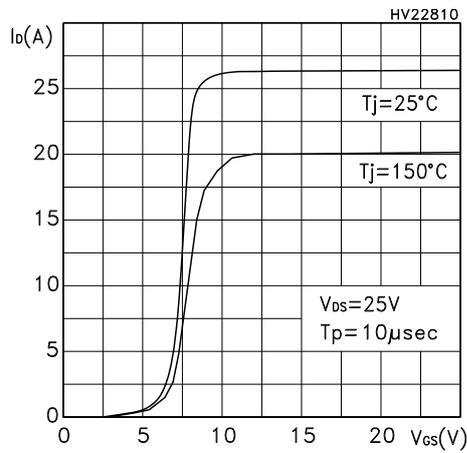
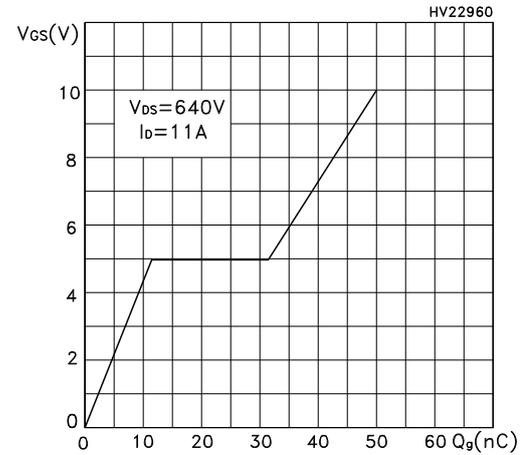
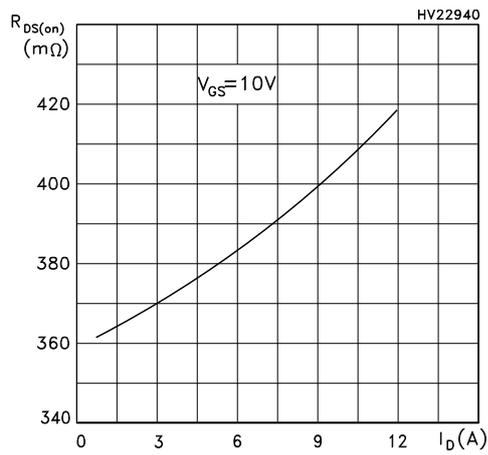
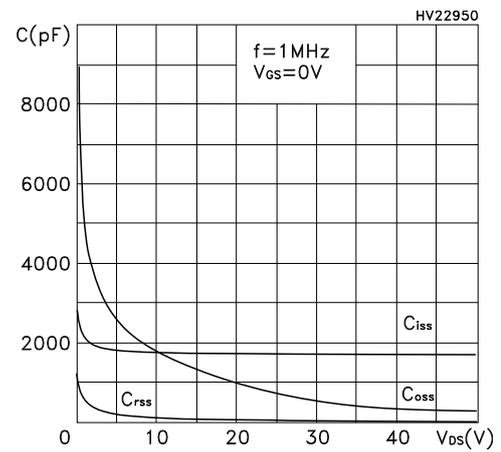
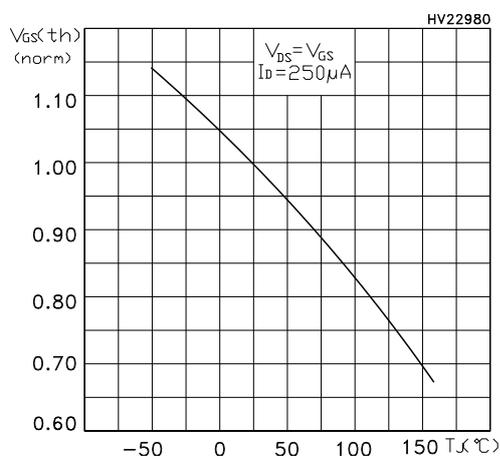
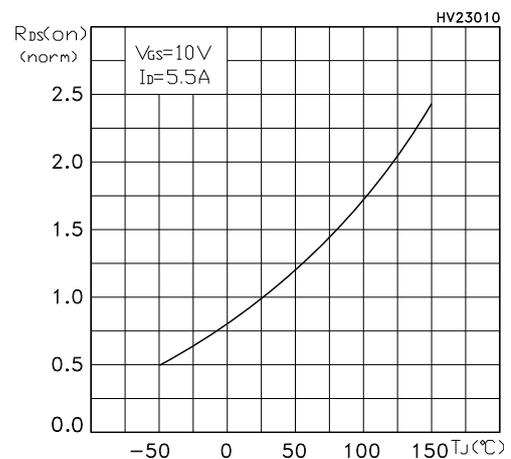
Figure 7. Typical transfer characteristics

Figure 8. Typical gate charge characteristics

Figure 9. Typical drain-source on-resistance

Figure 10. Typical capacitance characteristics

Figure 11. Normalized gate threshold vs temperature

Figure 12. Normalized on-resistance vs temperature


Figure 13. Normalized breakdown voltage vs temperature

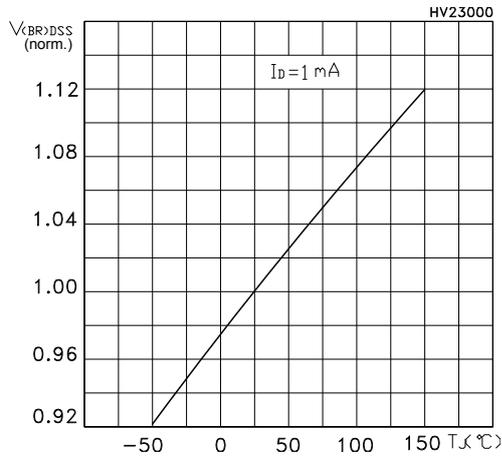
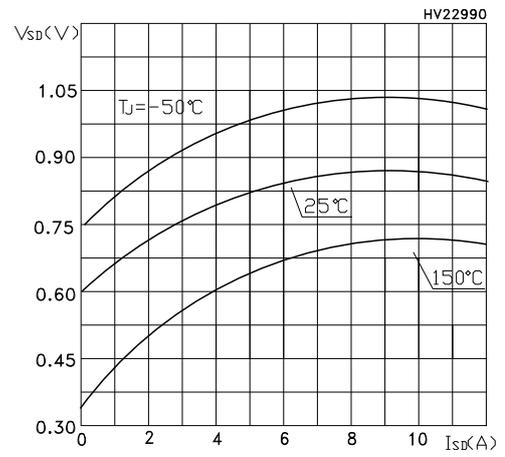
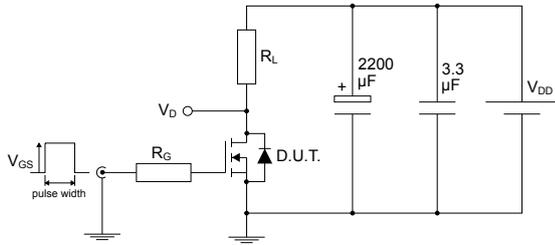


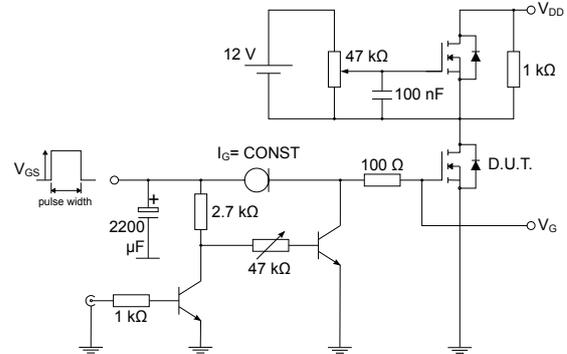
Figure 14. Typical reverse diode forward characteristics



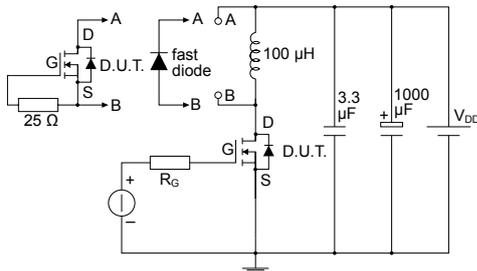
3 Test circuits

Figure 15. Test circuit for resistive load switching times


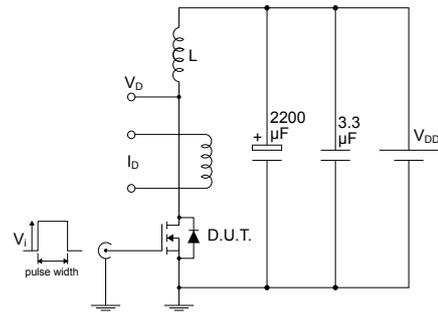
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Figure 16. Test circuit for gate charge behavior


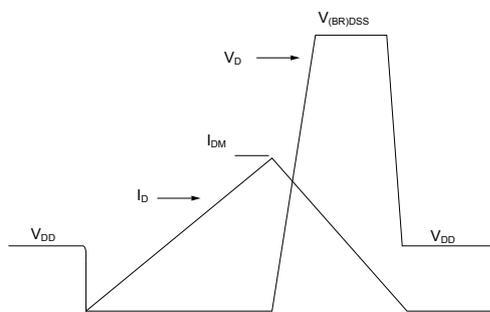
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Figure 17. Test circuit for inductive load switching and diode recovery times


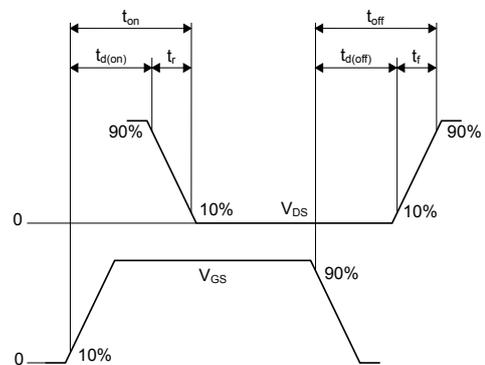
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Figure 18. Unclamped inductive load test circuit


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Figure 19. Unclamped inductive waveform


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Figure 20. Switching time waveform


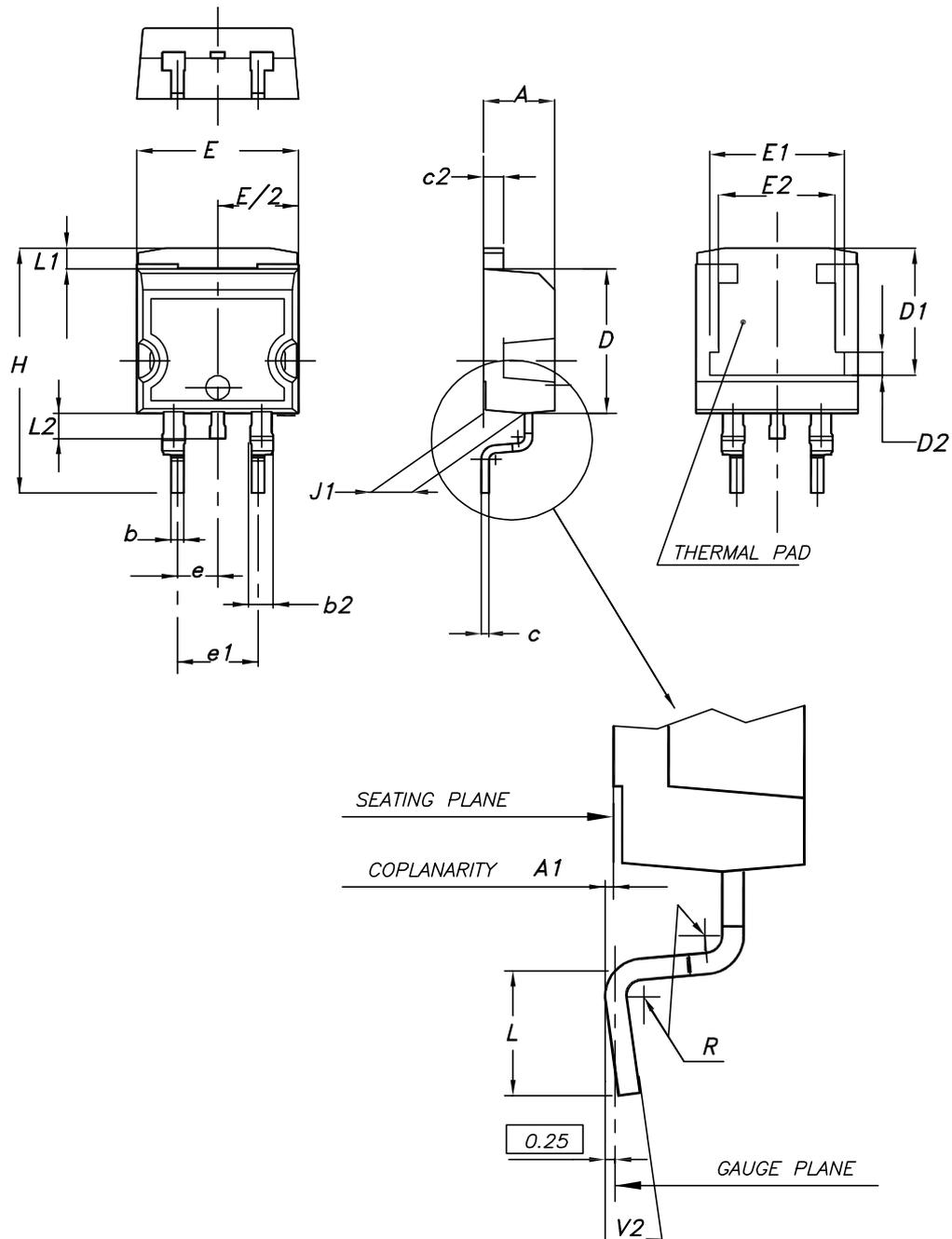
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 21. D²PAK (TO-263) type A package outline

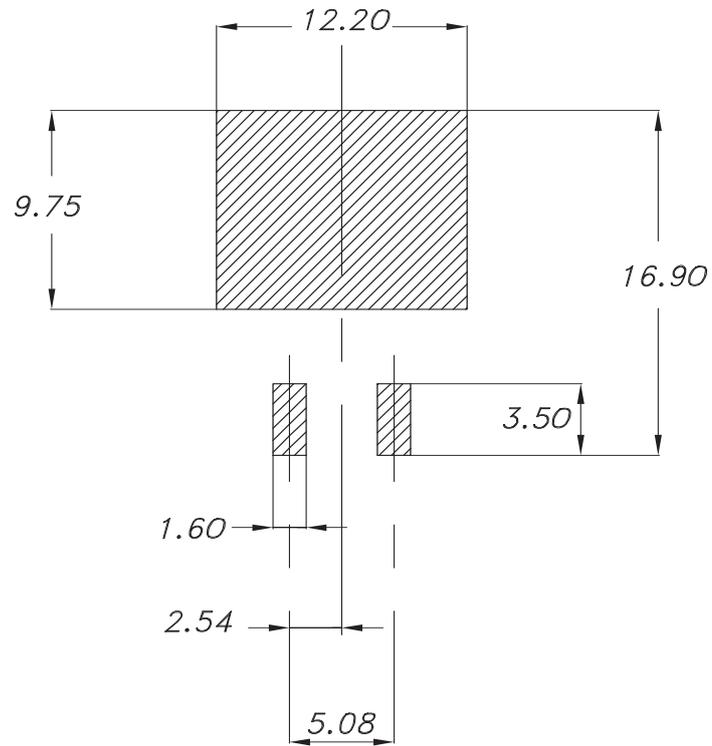


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Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

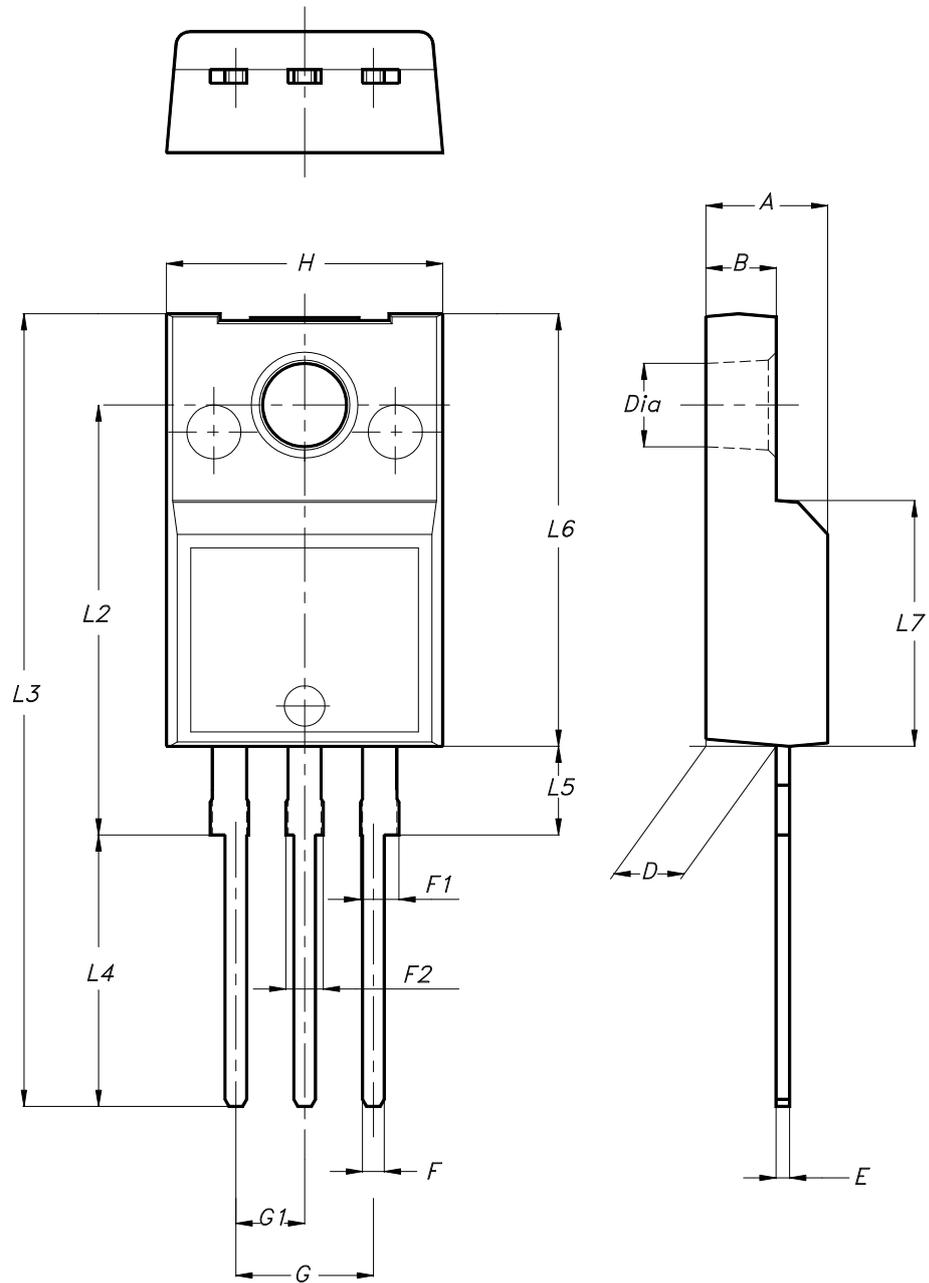
Figure 22. D²PAK (TO-263) recommended footprint (dimensions are in mm)



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4.2 TO-220FP type B package information

Figure 23. TO-220FP type B package outline



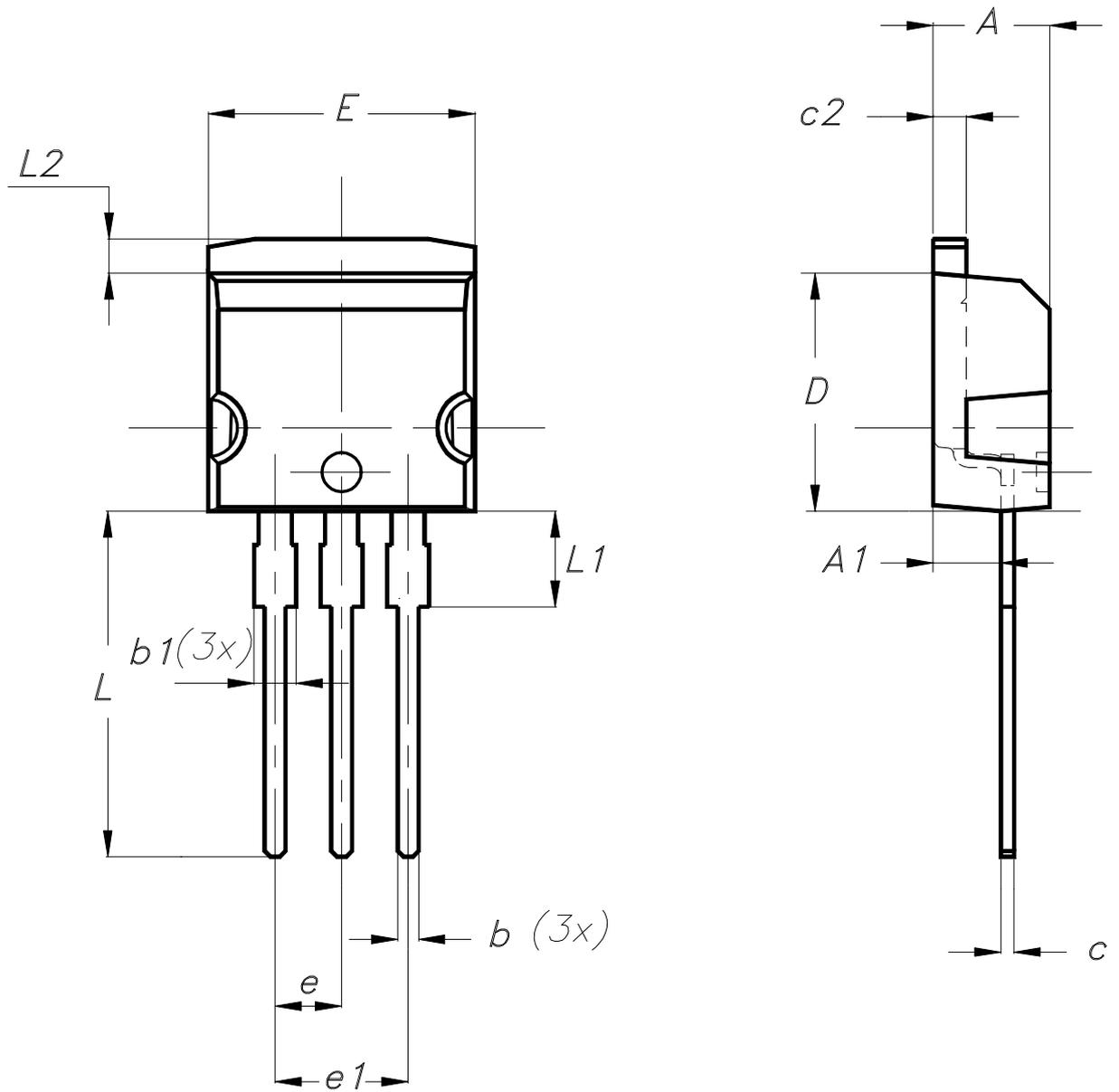
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Table 9. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.3 I²PAK package information

Figure 24. I²PAK package outline



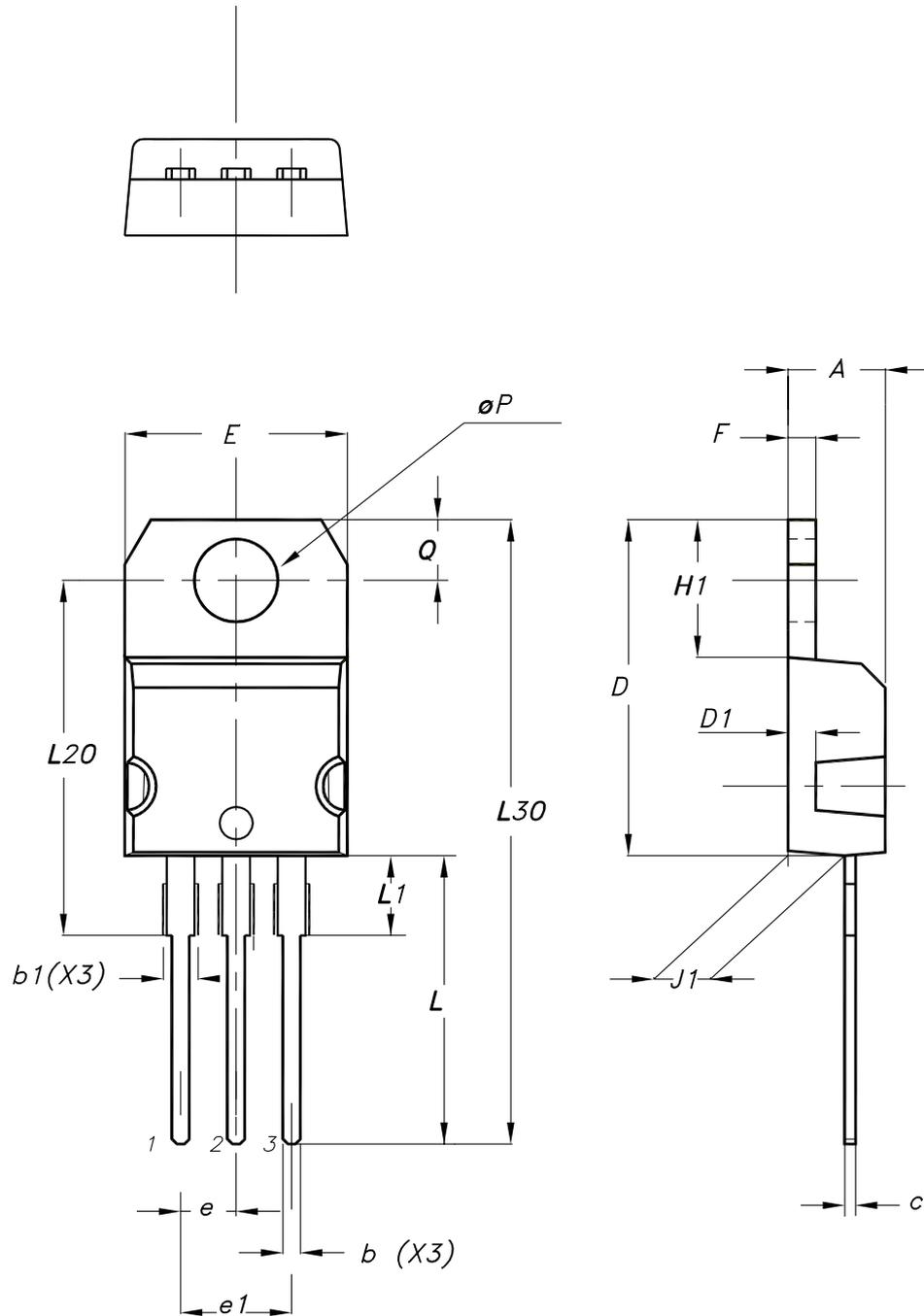
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Table 10. I²PAK package mechanical data

Dim.	mm	
	Min.	Max.
A	4.40	4.60
A1	2.40	2.72
b	0.61	0.88
b1	1.14	1.70
c	0.49	0.70
c2	1.23	1.32
D	8.95	9.35
e	2.40	2.70
e1	4.95	5.15
E	10.00	10.40
L	13.00	14.00
L1	3.50	3.93
L2	1.27	1.40

4.4 TO-220 type A package information

Figure 25. TO-220 type A package outline



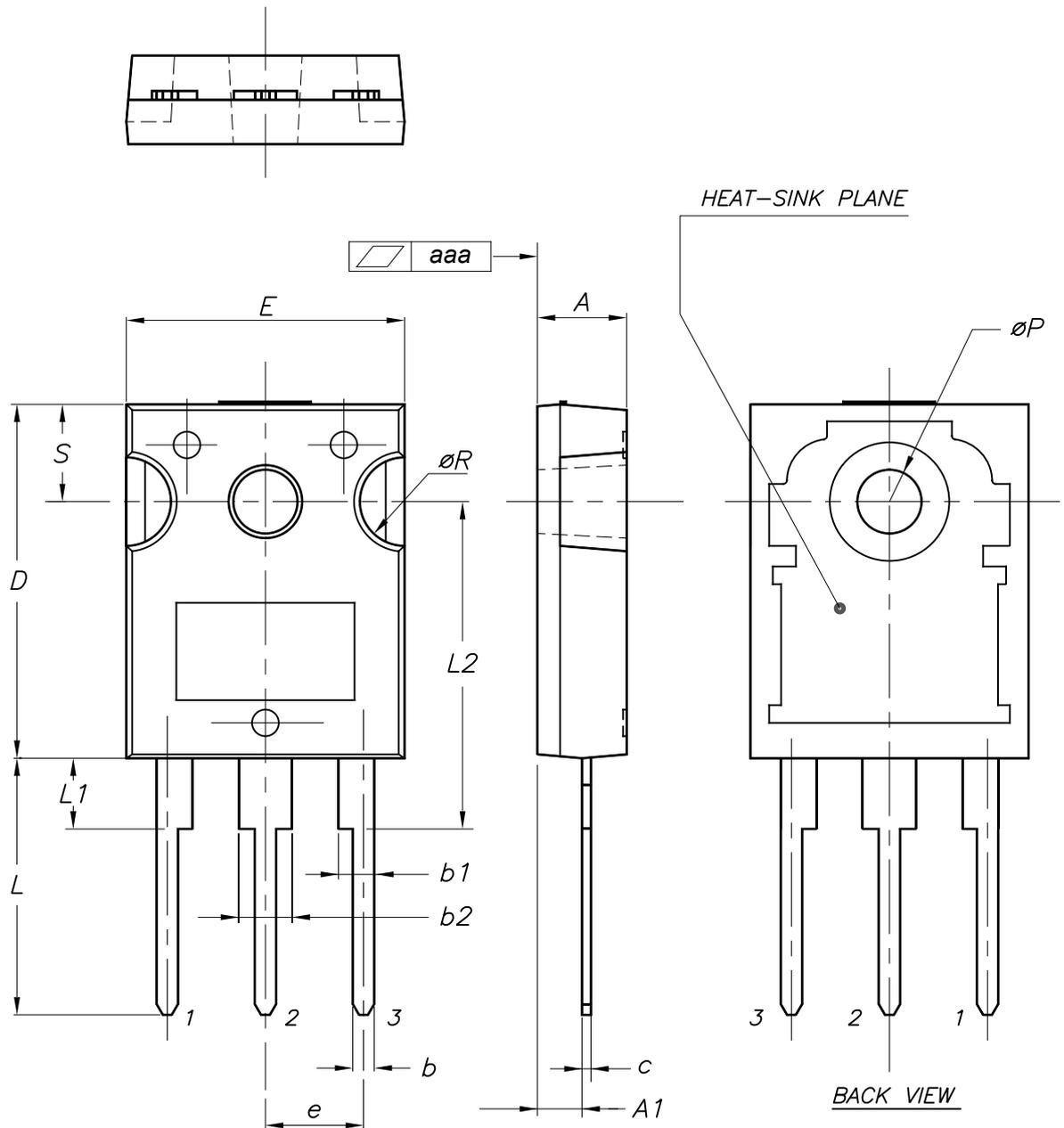
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Table 11. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.5 TO-247 package information

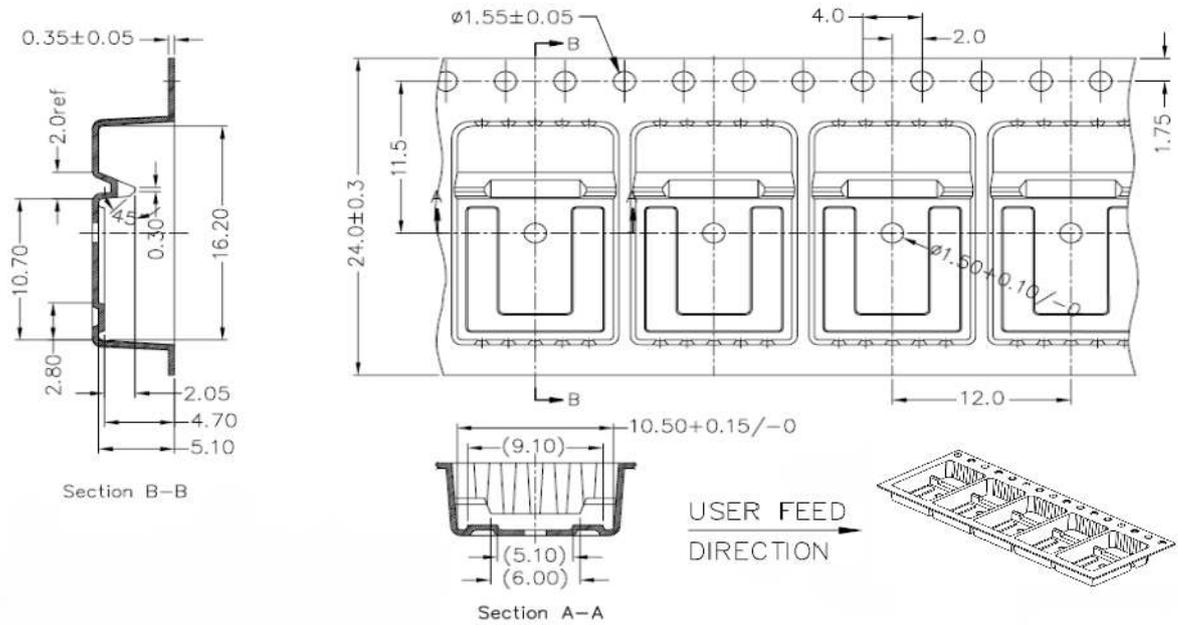
Figure 26. TO-247 package outline



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Table 12. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

4.6 D²PAK packing information
Figure 27. D²PAK tape drawing (dimensions are in mm)


DM01095771_2



5 Ordering information

Table 13. Order codes

Order codes	Marking	Package	Packing
STB11NM80T4	B11NM80	D ² PAK	Tape and reel
STF11NM80	F11NM80	TO-220FP	Tube
STI11NM80	I11NM80	I ² PAK	
STP11NM80	P11NM80	TO-220	
STW11NM80	W11NM80	TO-247	

Revision history

Table 14. Document revision history

Date	Revision	Changes
30-Sep-2004	4	Preliminary version
26-Nov-2005	5	Complete version
07-Apr-2006	6	Modified value on <i>Figure 8</i>
15-May-2006	7	New dv/dt value on <i>Table 5</i>
20-Jul-2006	8	The document has been reformatted
20-Dec-2007	9	Updated I_D value on <i>Table 2: Absolute maximum ratings</i>
24-Mar-2010	10	Inserted dv/dt value in <i>Table 2: Absolute maximum ratings</i>
12-Sep-2011	11	Added new package and mechanical data : I ² PAK Minor text changes
17-Sep-2025	12	Updated Section 4: Package information . Minor text changes.



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4.3	I ² PAK package information	14
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