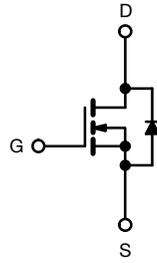
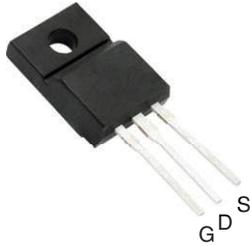


## Power MOSFET

**TO-220 FULLPAK**


N-Channel MOSFET

### FEATURES

- Low gate charge  $Q_g$  results in simple drive requirement
- Improved gate, avalanche and dynamic  $dV/dt$  ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective  $C_{oss}$  specified
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT

### APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching
- High voltage isolation = 2.5 kV<sub>RMS</sub> (t = 60 s, f = 60 Hz)

### TYPICAL SMPS TOPOLOGIES

- Two transistor forward
- Half and full bridge convertors
- Power factor correction boost

### PRODUCT SUMMARY

$V_{DS}$ (V)	500	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	0.52
$Q_g$ (Max.) (nC)	52	
$Q_{gs}$ (nC)	13	
$Q_{gd}$ (nC)	18	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	IRFIB7N50APbF

### ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	500	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current <sup>f</sup>	$I_D$	$T_C = 25$ °C	A
Continuous drain current		$T_C = 100$ °C	
Pulsed drain current <sup>a, e</sup>	$I_{DM}$	44	
Linear derating factor		0.48	W/°C
Single pulse avalanche energy <sup>b, e</sup>	$E_{AS}$	275	mJ
Repetitive avalanche current <sup>a, e</sup>	$I_{AR}$	11	A
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	6.0	mJ
Maximum power dissipation	$P_D$	60	W
Peak diode recovery $dV/dt$ <sup>c, e</sup>	$dV/dt$	6.9	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300	
Mounting torque	M3 screw	0.6	Nm

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting  $T_J = 25$  °C,  $L = 4.5$  mH,  $R_G = 25$   $\Omega$ ,  $I_{AS} = 11$  A (see fig. 12)
- $I_{SD} \leq 11$  A,  $dI/dt \leq 140$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C
- 1.6 mm from case
- Uses IRFB11N50A, SiHFB11N50A data and test conditions
- Drain current limited by maximum junction temperature

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	65	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	2.1	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		500	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}^d$		-	610	-	mV/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 4.0\text{ A}^b$	-	-	0.52	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 6.6\text{ A}^d$		6.1	-	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$ , see fig. 5 <sup>d</sup>		-	1423	-	pF
Output capacitance	$C_{oss}$			-	208	-	
Reverse transfer capacitance	$C_{rss}$			-	8.1	-	
Output capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	2000	-	pF
			$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	55	-	
Effective output capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 400\text{ V}^{c, d}$		-	97	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 11\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 <sup>b, d</sup>	-	-	52	nC
Gate-source charge	$Q_{gs}$			-	-	13	
Gate-drain charge	$Q_{gd}$			-	-	18	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 11\text{ A}$ $R_G = 9.1\text{ }\Omega, R_D = 22\text{ }\Omega,$ see fig. 10 <sup>b, d</sup>		-	14	-	ns
Rise time	$t_r$			-	35	-	
Turn-off delay time	$t_{d(off)}$			-	32	-	
Fall time	$t_f$			-	28	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode		-	-	6.6	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$			-	-	44	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 11\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 11\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^{b, d}$		-	510	770	ns
Body diode reverse recovery charge	$Q_{rr}$			-	3.4	5.1	$\mu\text{C}$
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$
- $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0% to 80%  $V_{DS}$
- Uses IRFB11N50A, SiHFB11N50A data and test conditions



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

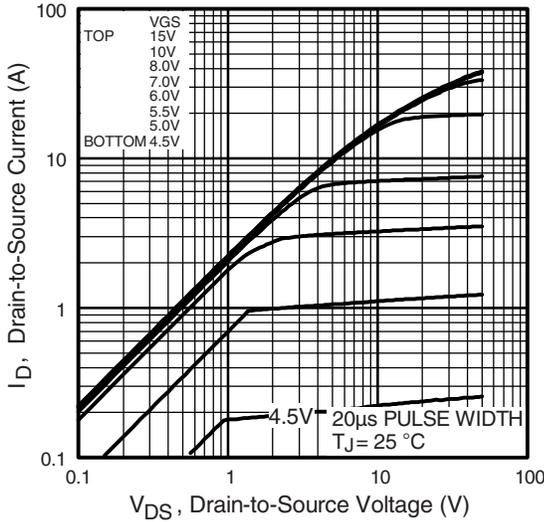


Fig. 1 - Typical Output Characteristics

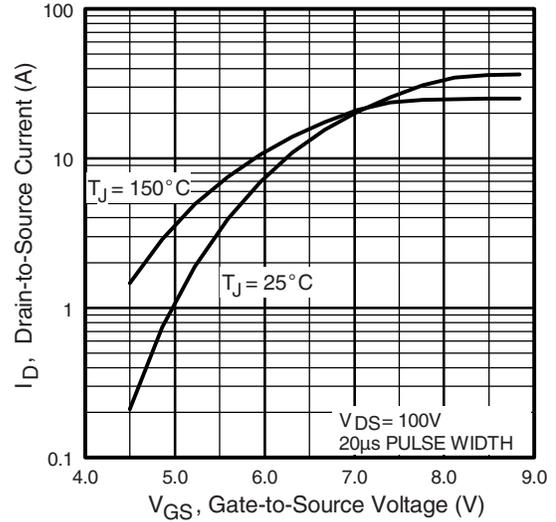


Fig. 3 - Typical Transfer Characteristics

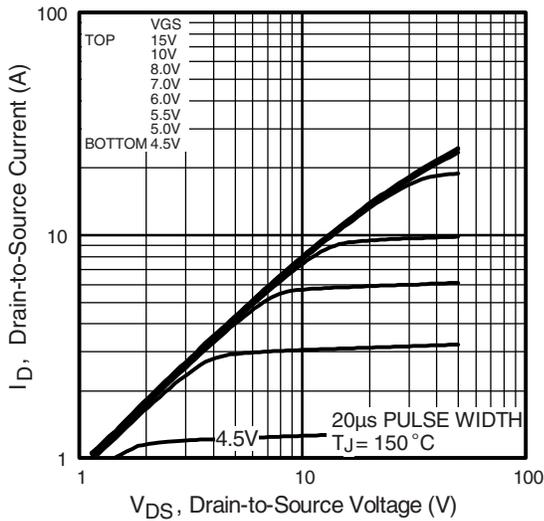


Fig. 2 - Typical Output Characteristics

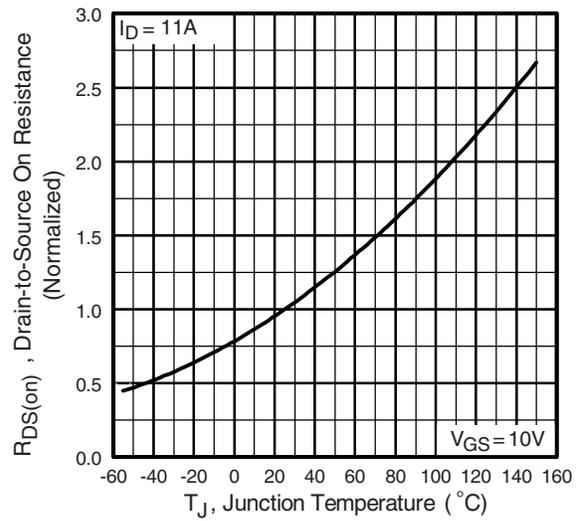


Fig. 4 - Normalized On-Resistance vs. Temperature

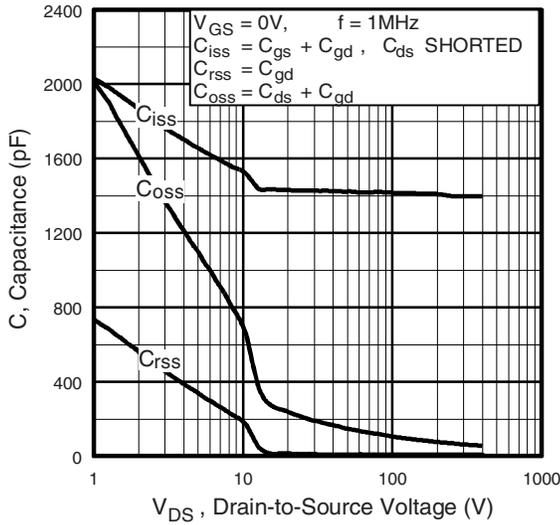


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

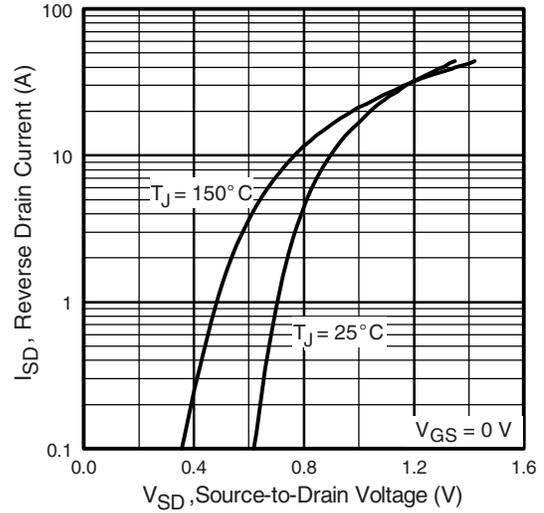


Fig. 7 - Typical Source-Drain Diode Forward Voltage

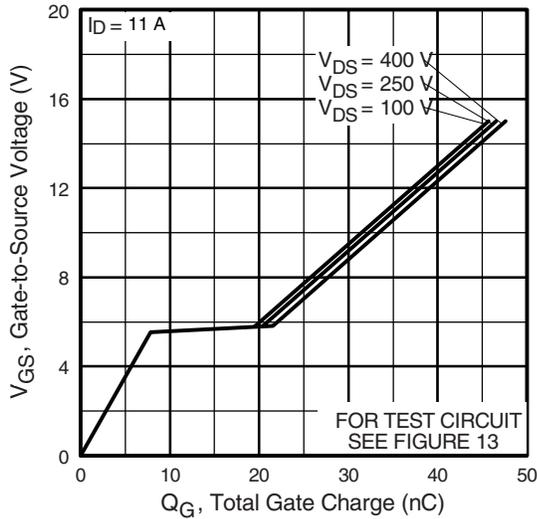


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

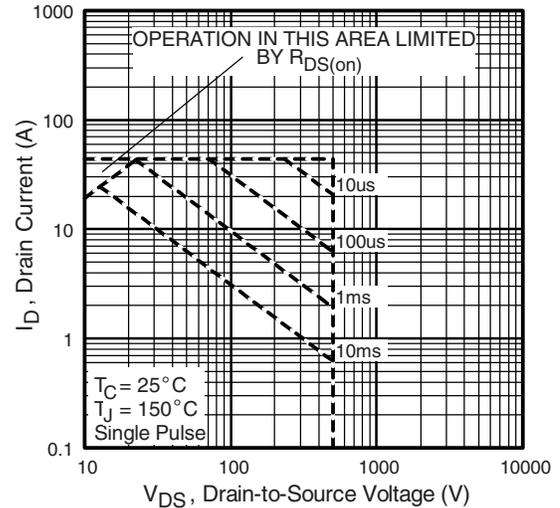


Fig. 8 - Maximum Safe Operating Area

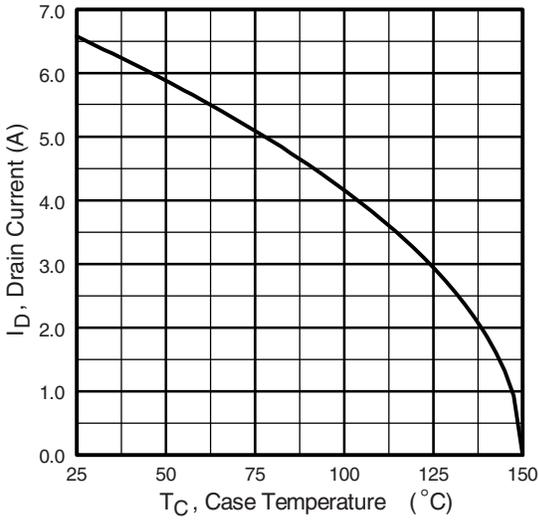


Fig. 9 - Maximum Drain Current vs. Case Temperature

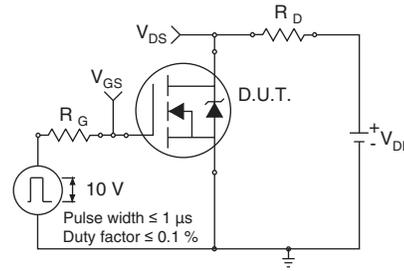


Fig. 10a - Switching Time Test Circuit

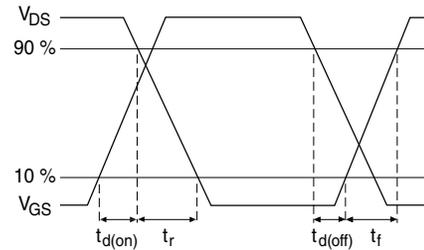


Fig. 10b - Switching Time Waveforms

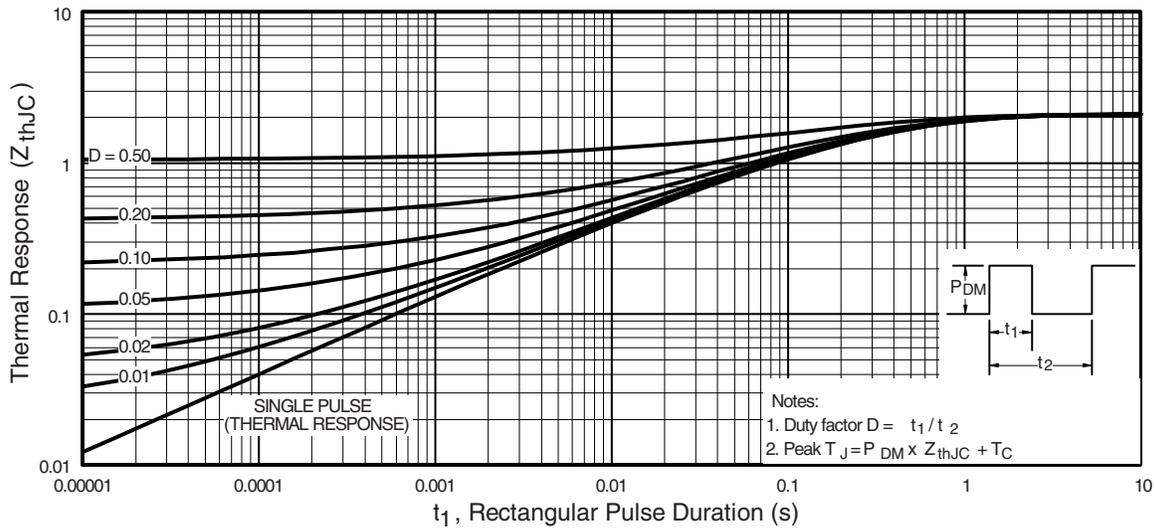


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

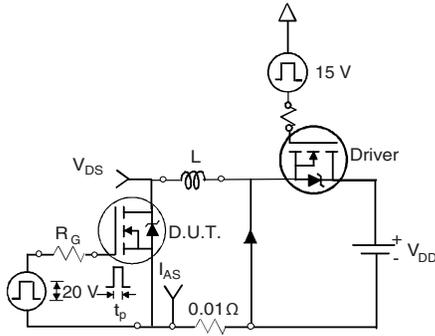


Fig. 12a - Unclamped Inductive Test Circuit

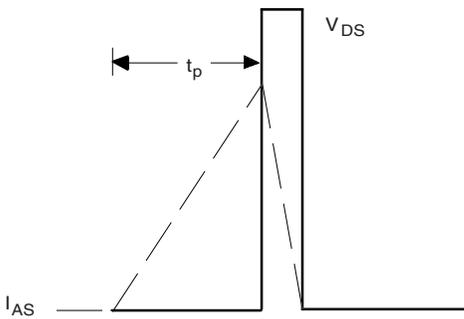


Fig. 12b - Unclamped Inductive Waveforms

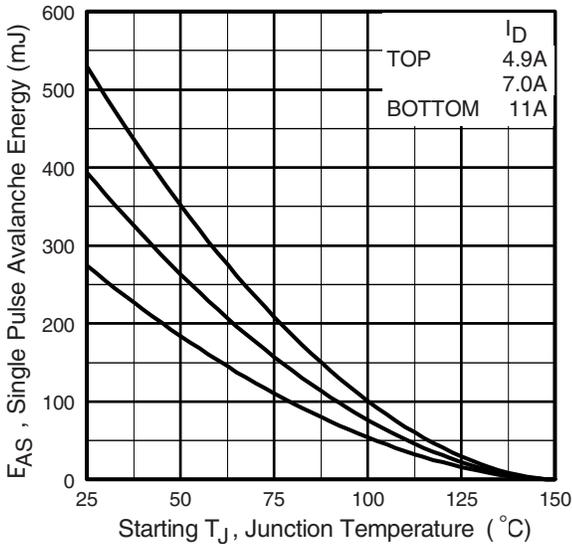


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

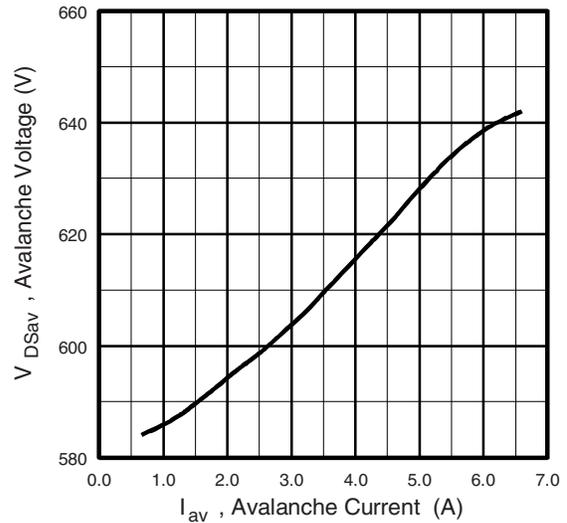


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

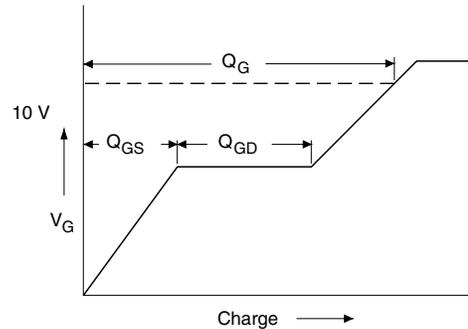


Fig. 13a - Basic Gate Charge Waveform

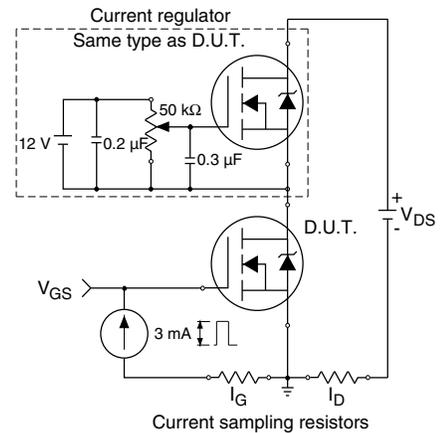
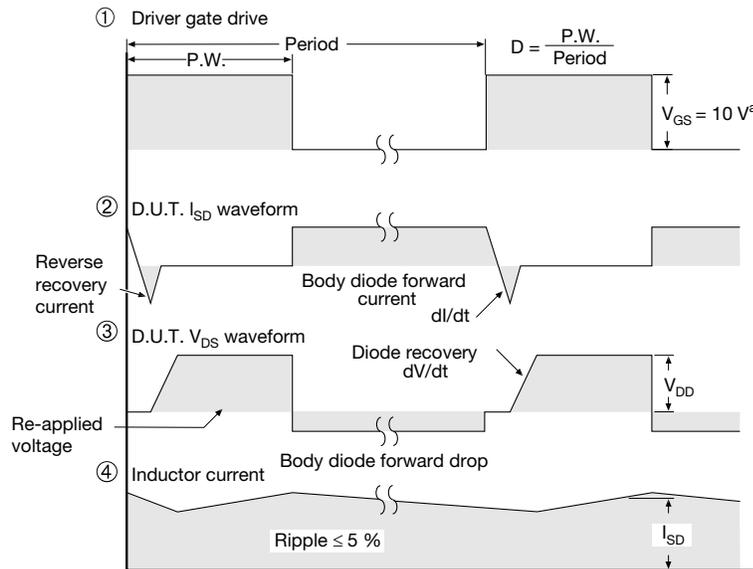
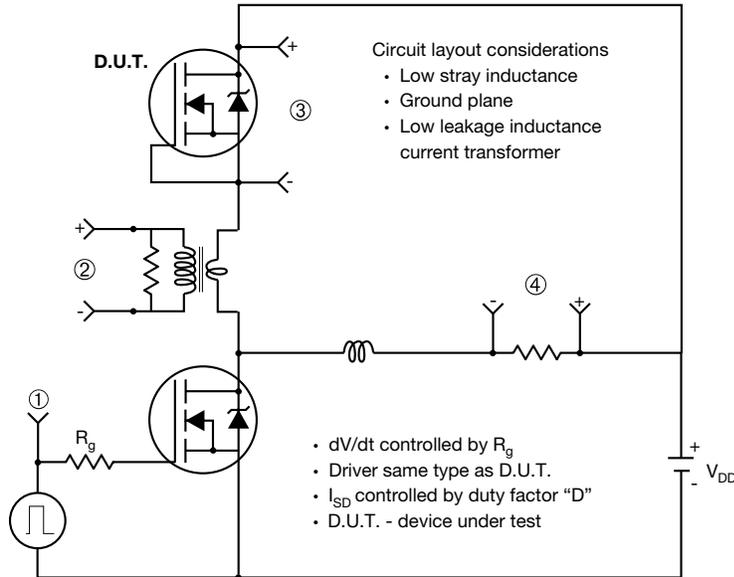


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a.  $V_{GS} = 5\text{ V}$  for logic level devices

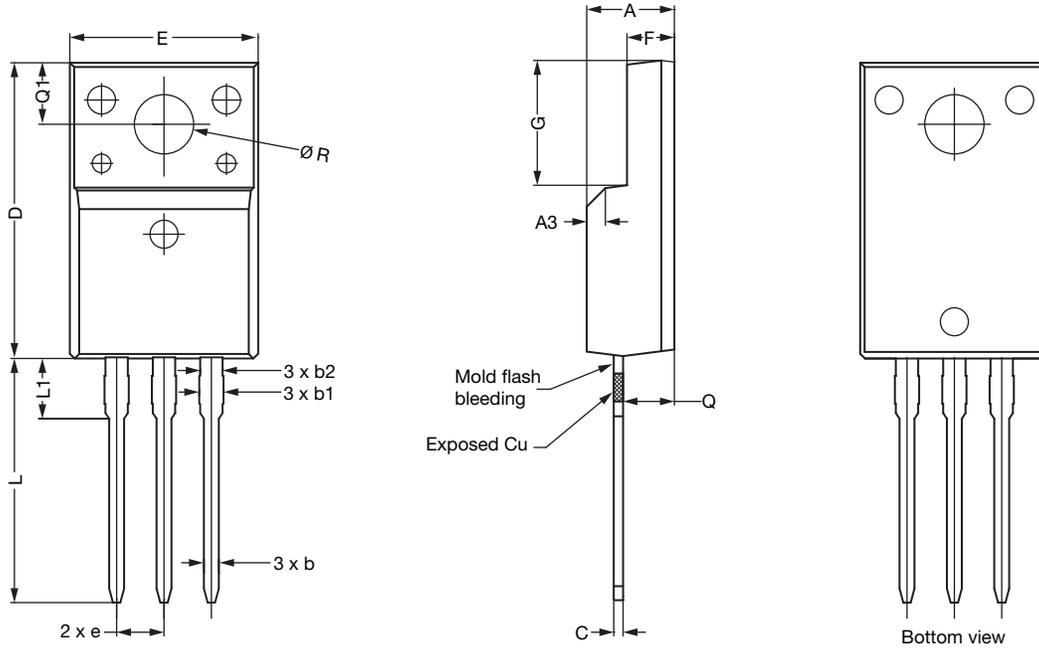
Fig. 14 - For N-Channel

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# TO-220 FULLPAK (High Voltage)

## OPTION 1: FACILITY CODE = 9



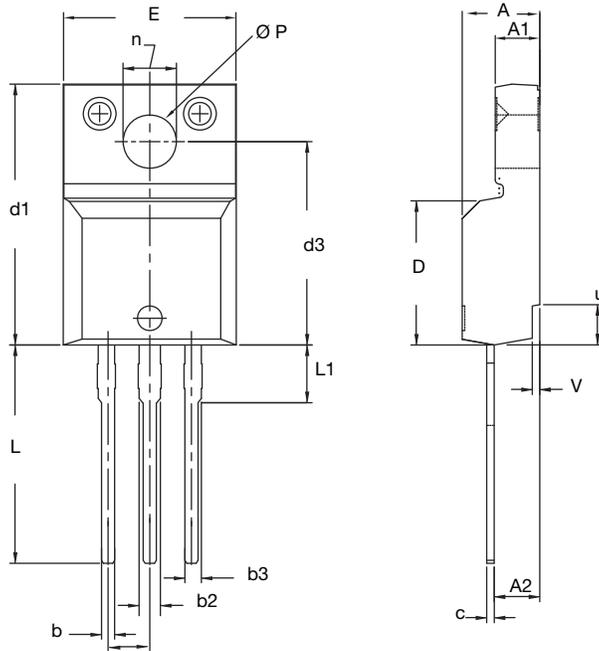
DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
$\varnothing R$	3.08	3.18	3.28

### Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking



OPTION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019  
DWG: 5972

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
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6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking



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