DIO4483/4483B

USB Type-C Analog Audio Switch with Protection Function and Comparator

Features

- Power supply voltage range: 2.55 V to 5.5 V
- Version information:
  - DIO4483: default: DP_R~DP; DN_L~DN; SBU1~SBU1_H; SBU2~SBU2_H turn on
  - DIO4483B: default: DP_R~DP; DN_L~DN turn on
- USB 2.0 high speed switch:
  - −3 dB bandwidth: 950 MHz
  - 4.6 Ω R_{ON} typical
- Audio switch
  - Negative rail capability: −3.6 V to 3.6 V
  - THD+N = -110 dB, 1 V_{RMS},
  - f = 20 Hz ~ 20 kHz,
  - 32 Ω load
  - −3 dB bandwidth: 800 MHz
  - 1.2 Ω R_{ON} typical
- UART high speed switch:
  - −3 dB bandwidth: 800 MHz
  - 10 Ω R_{ON} typical
- High voltage protection
  - +20 V DC tolerance on USB Type-C pins
  - ±25 V surge capable on USB Type-C pins
  - ±5 kV HBM ESD
- Over voltage protection:
  - DP_R, DN_L, SBU1/SBU2/GSBU1/GSBU2 V_{TH} = 4.4 V (default), 4.4 V ~ 5.0 V configurable, 0.2 V/step
- Support OMTP, CTIA and 3-pole audio jack pinout
- Built-in comparator, normally active
- 25-ball WLCSP package

Applications

- Mobile phones
- Tablets
- Notebook PCs
- Media players

Descriptions

The DIO4483/4483B is a high-performance USB Type-C analog switch for use in portable multimedia devices, supporting analog audio headsets. The DIO4483/4483B can detect OMTP, CTIA, or 3-pole headsets and configure pinouts automatically. The DIO4483/4483B shares common Type-C pins to pass USB 2.0 signals and analog audio signals; the sideband uses wires and analog microphone signals. The DIO4483/4483B also supports high voltage and surge on SBUx pins and USB pins on the USB Type-C receptacle side. The internal ultra-low power comparator has a typical power supply current of 0.3 μA. It has the best-in-class power supply current versus propagation delay performance. Featuring a push-pull output stage, the comparator allows operation with the absolute minimum power consumption when driving any capacitive or resistive load.

Block Diagram

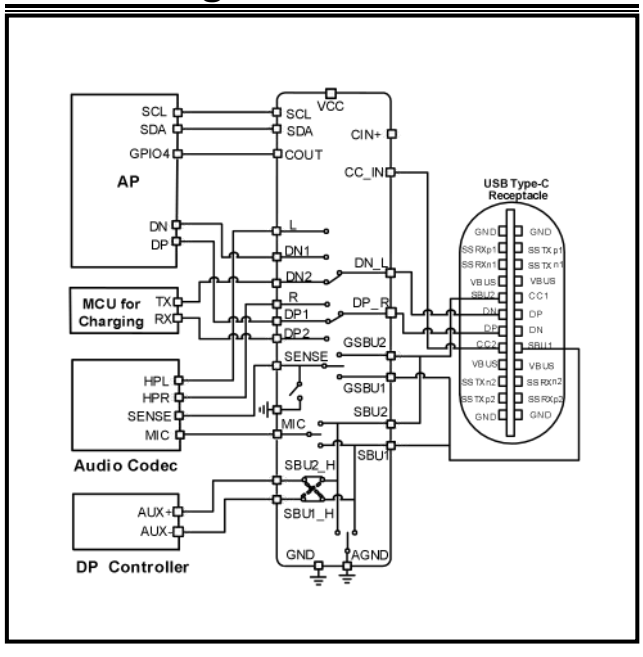


Figure 1. Application block diagram

Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO4483WL25	D4HC	1	Green	-40 to 85°C	WLCSP-25	Tape & Reel, 3000
DIO4483BWL25	DH3B	1	Green	-40 to 85°C	WLCSP-25	Tape & Reel, 3000

Pin Assignment

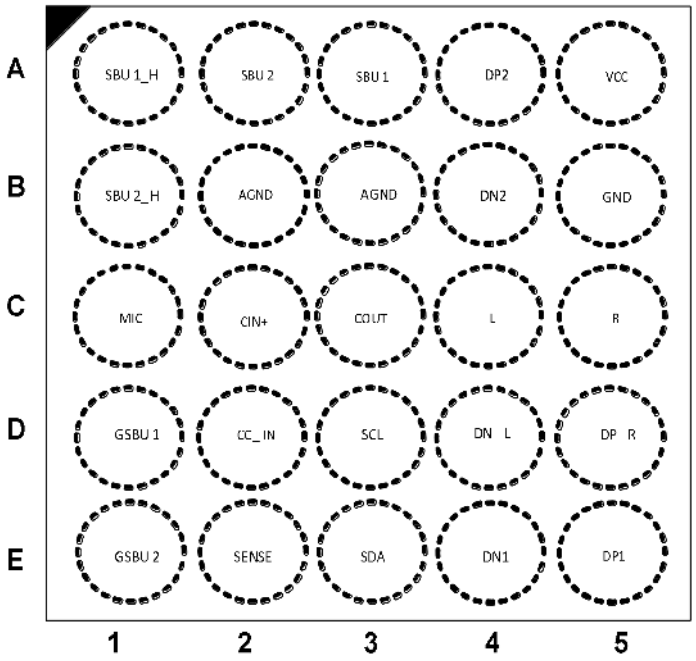


Figure 2. WLCSP-25 (Top view)

Pin Descriptions

Pin	Name	Description
A5	VCC	Power supply (2.55 to 5.5 V)
B5	GND	Chip ground
D5	DP_R	USB/Audio common pin
D4	DN_L	USB/Audio common pin
E5	DP1	USB data1 (differential +)
E4	DN1	USB data1 (differential –)
C5	R	Audio – right channel
C4	L	Audio – left channel
A3	SBU1	Sideband use wire 1
A2	SBU2	Sideband use wire 2
C1	MIC	Microphone signal
B2	AGND	Audio signal ground
B3	AGND	Audio signal ground
E2	SENSE	Audio ground reference output
C3	COUT	Open-drain comparator OUT.
D2	CC_IN	Audio accessory attachment detection input
D1	GSBU1	Audio sense path 1 to headset jack GND
E1	GSBU2	Audio sense path 2 to headset jack GND
C2	C1N+	Comparator IN+
D3	SCL	I^2C clock
E3	SDA	I^2C data
B1	SBU2_H	Host side sideband use wire 2
A1	SBU1_H	Host side sideband use wire 1
A4	DP2	USB data2 (differential +)
B4	DN2	USB data2 (differential –)

Absolute Maximum Ratings

Stresses beyond those listed under the Absolute Maximum Rating table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage from V_{CC}		-0.5	6.5	V
V_{CC_IN}	V_{CC_IN}, to GND		-0.5	20	V
V_{SW_C}	V_{DP_R} to GND, V_{DN_L} to GND		-3.5	20	V
V_{SW_USB}	V_{DP1} to GND, V_{DN1} to GND		-0.5	6.5	V
V_{SW_Audio}	V_L to GND, V_R to GND		-3.6	6.5	V
V_{SW_UART}	V_{DP2} to GND, V_{DN2} to GND		-3.6	6.5	V
$V_{V\_SBUx/GSBUx}$	V_{SBU1} to GND, V_{SBU2} to GND, V_{GSBU1} to GND, V_{GSBU1} to GND		-0.5	20	V
V_{VSBUx_H}	V_{SBU1_H} to GND, V_{SBU2_H} to GND		-0.5	6.5	V
$V_{I/O}$	SENSE, MIC, to GND		-0.5	6.5	V
V_{CNTRL}	Control input voltage	SDA, SCL	-0.5	6.5	V
$V_{comparator}$	Comparator input and output	CIN+, COUT	-0.5	6.5	V
I_{SW_Audio}	Switch I/O current, audio path		-250	250	mA
I_{SW_USB}	Switch I/O current, USB path		–	100	mA
I_{SW_MIC}	Switch I/O current, MIC to SBU1 or SBU2		–	50	mA
I_{SW_SBUx}	Switch I/O current, SBUx to SBUx_H		–	50	mA
I_{SW_SENSE}	Switch I/O current, SENSE to GSBU1 or GSBU2		–	100	mA
I_{SW_AGND}	Switch I/O current, AGND to SBU1 or SBU2		–	500	mA
I_{IK}	DC input diode current		-50	–	mA
ESD	Human body model, ANSI/ESDA/JEDEC JS−001		±5	–	kV
	Charged device model, ANSI/ESDA/JEDEC JS−002		±2	–	kV
Latch-up			200	–	mA
T_A	Absolute maximum operating temperature		-40	85	°C
T_{STG}	Storage temperature		-65	150	°C

Recommend Operating Conditions

Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min	Typ	Max	Unit
Power					
V_{CC}	Supply voltage	2.55	–	5.5	V
USB switch					
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND, V_{DP_R} to GND, V_{DN_L} to GND	0	–	3.6	V
Audio switch					
V_{SW_Audio}	V_{DP_R} to GND, V_{DN_L} to GND, V_L to GND, V_R to GND	−3.6	–	3.6	V
MIC switch					
V_{VSBU_MIC}	V_{SBU1} to GND, V_{SBU2} to GND, V_{MIC} to GND	0	–	3.6	V
SENSE switch					
V_{VGSBU_SEN}	V_{GSBU1} to GND, V_{GSBU2} to GND, V_{SENSE} to GND	0	–	3.6	V
SBU to SBUX_H switch					
V_{VGSBU}	V_{SBU1} to GND, V_{SBU2} to GND, V_{SBU1_H} to GND, V_{SBU2_H} to GND	0	–	3.6	V
CC_IN pin					
V_{CC_IN}	V_{CC_IN} to GND	0	–	5.5	V
Control voltage (SDA/SCL)					
V_{IH}	Input voltage high	0.825	–	V_{CC}	V
V_{IL}	Input voltage low	–	–	0.3	V
Operating temperature					
T_A	Ambient operating temperature	−40	25	85	°C
Comparator					
Supply voltage		2.55		5.5	V
Quiescent current	T_A = 25°C	500 (max)			nA
	T_A = –40°C to 125°C	1000 (max)			nA

DC Electrical Characteristics

V_{CC} = 2.55 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Power	Min	Typ	Max	Unit
I_{CC}	Supply current	USB switches on, SBUx to SBUx_H switches on	V_{CC} = 4.2 V		55		μA
		Audio switches on, MIC switch on and Audio GND switch on			53		μA
I_{CCZ}	Quiescent current	04H'b7 = 0			4		μA
USB/Audio common pins: DP_R, DN_L							
I_{OZ}	Off leakage current of DP_R and DN_L	DN_L, DP_R = −3 V to 3.6 V	V_{CC} = 2.55 V to 5.5 V	-3		3	μA
I_{OFF}	Power−off leakage current of DP_R and DN_L	DN_L, DP_R = 0 V to 3.6 V	Power off	-3		3	μA
V_{OV_TRIP}	Input OVP lockout	Rising edge	V_{CC} = 2.55 V to 5.5 V	4.2	4.4	4.6	V
V_{OV_HYS}	Input OVP hysteresis				0.24		V
Audio switch							
I_{ON}	On leakage current of audio switch	DN_L, DP_R = −3 V to 3 V, DP, DN, R, L = Float	V_{CC} = 2.55 V to 5.5 V	-3		3	μA
I_{OFF}	Power−off leakage current of L and R	L, R = 0 V to 3 V; DP_R, DN_L = Float	Power off	-1		1	μA
R_{ON}	Switch on resistance	I_{SW} = 100 mA, V_{SW} = −3 V to 3 V	V_{CC} = 2.55 V to 5.5 V		1.2		Ω
R_{SHUNT}	Pull-down resistor on R/L pin when audio switch is off	L= R = 3 V		6	10	14	kΩ
USB switch							
I_{ON}	On leakage current of USB switch	DN_L, DP_R = 0 V to 3.6 V, DP, DN, R, L = Float	V_{CC} = 2.55 V to 5.5 V	-3		3	μA
I_{OZ}	Off leakage current of DP and DN	DN, DP = 0 V to 3.6 V		-3		3	μA
I_{OFF}	Power−off leakage current of DP and DN	DN, DP = 0 V to 3.6 V	Power off	-3		3	μA
R_{ON_USB}	USB switch on resistance	I_{SW} = 8 mA, V_{SW} = 0.4 V	V_{CC} = 2.55 V to 5.5 V		4.6		Ω
UART switch							
I_{OZ}	Off leakage current of DP and DN	DN, DP = 0 V to 3.6 V		-3		3	μA
I_{OFF}	Power−off leakage current of DP and DN	DN, DP = 0 V to 3.6 V	Power off	-3		3	μA

R_{ON_UART}	UART switch on resistance	I_{SW} = 3 mA, V_{SW} = 0.4 V	V_{CC} = 2.55 V to 5.5 V		10		Ω
I_{ON}	On leakage current UART switch	DP2 = DN2 = 3.6 V	V_{CC} = 2.55 V to 5.5 V		1.35		uA
SENSE-AGND switch							
R_{ON}	SENSE switch on resistance	I_{OUT} = 100 mA, V_{SW} = 1.0 V	V_{CC} = 2.55 V to 5.5 V		8		Ω
SENSE switch							
I_{ON}	Sense path leakage current	GSBUx = 0 V to 1 V, SENSE is floating	V_{CC} = 2.55 V to 5.5 V	-2		2	μA
R_{ON}	SENSE switch on resistance	I_{OUT} = 100 mA, V_{SW} = 1.0 V	V_{CC} = 2.55 V to 5.5 V		330		mΩ
I_{OFF}	Power−off leakage current of SENSE	Sense = 0 V to 1.0 V	V_{CC} = 2.55 V to 5.5 V	-2		2	μA
	Power−off leakage current of GSBUx	GSBUx = 0 V to 3.6 V		-3		3	μA
V_{OV_TRIP}	Input OVP lockout on GSBUx	Rising edge	V_{CC} = 2.55 V to 5.5 V	4.2	4.4	4.6	V
V_{OV_HYS}	Input OVP hysteresis of GSBUx				0.24		V
SBUX pins							
I_{OZ}	Off leakage current of SBUx	SBUx = 0 V to 3.6 V	V_{CC} = 2.55 V to 5.5 V	-3		3	μA
I_{OFF}	Power−off leakage current port SBUx	SBUx = 0 V to 3.6 V	Power off	-2		10	μA
V_{OV_TRIP}	Input OVP lockout	Rising edge	V_{CC} = 2.55 V to 5.5 V	4.2	4.4	4.6	V
V_{OV_HYS}	Input OVP hysteresis				0.24		V
MIC switch							
I_{ON}	On leakage current of MIC switch	SBUx = 0 V to 3.6 V, MIC is floating	V_{CC} = 2.55 V to 5.5 V	-3		3	μA
I_{OZ}	Off leakage current of MIC	MIC = 0 V to 3.6 V		-1		1	μA
I_{OFF}	Power-off leakage current of MIC	MIC = 0 V to 3.6 V	Power off	-1		1	μA
R_{ON}	MIC switch on resistance	V_{SW} = 3.6 V, I_{SW} = 30 mA	V_{CC} = 2.55 V to 5.5 V		3.1		Ω
SBUX_H switch							
I_{ON}	On leakage current of SBUx_H switch	SBUx = 0 V to 3.6 V, SBUx_H is floating	V_{CC} = 2.55 V to 5.5 V	-3		3	μA
I_{OZ}	Off leakage of SBUx_H	SBUx_H = 0 V to 3.6 V		-1		1	μA
I_{OFF}	Power off leakage current of SBUx_H	SBUx_H = 0 V to 3.6 V	Power off	-1		1	μA

R_{ON}	SBUx_H switch on resistance	V_{SW} = 0 V to 3.6 V, I_{SW} = 30 mA	V_{CC} = 2.55 V to 5.5 V		2.8		Ω
Audio ground switch: pin: AGND to SBUX							
R_{ON}	AGND switch on resistance	I_{SOURCE} = 100 mA on SBUx	V_{CC} = 2.55 V to 5.5 V		66		mΩ
CC_IN pin							
V_{TH_L}	Input low threshold		V_{CC} = 2.55 V to 5.5 V		1.2		V
V_{TH_H}	Input high threshold				1.5		V
I_{IN}	Input leakage of CC_IN	CC_IN = 0 V to 5.5 V				1.0	μA
SDS, SCL pins							
V_{ILI2C}	Low−level input voltage		V_{CC} = 2.55 V to 5.5 V			0.3	V
V_{IHI2C}	High−level input voltage			0.825			V
I_{I2C}	Input current of SDA and SCL pins	SCL/SDA = 0 V to 3.6 V		-5		5	μA
V_{OLSDA}	Low−level output voltage	I_{OL} = 2 mA				0.3	V
I_{OLSDA}	Low−level output current	V_{OLSDA} = 0.2 V		10			mA
OVP (1)							
V_{OV_TRIP}	Input OVP lockout on receptacle side pin	Rising edge	V_{CC} = 2.55 V to 5.5 V	4.2	4.4	4.6	V
V_{OV_HYS}	Input OVP hysteresis of DP_R,DN_L,SBU$_X$, GSBUx on receptacle side pin				0.24		V

Note:

(1) The OVP voltage can be adjusted by bit [7:6] for 12h: 4.4 V, 4.6 V, 4.8 V, 5 V.

(2) Specificatons subject to change without notice.

Comparator Electrical Characteristics

At T_A = 25°C, V_{CC} = 2.55 V to 5 V, C_L = 15 pF, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Offset voltage						
V_{REF}	Reference voltage	T_A = 25°C to 65°C	218.5	225	231.5	mV
V_{HYS}	Hysteresis			30	40	mV
dV_{OS}/dT	Input offset voltage drift	T_A = -40°C to 125°C			±70	μV/°C
Input voltage range						
V_{CM}	Common-mode voltage range	T_A = -40°C to 125°C	- 0.1		V_{CC} + 0.1	V
Input bias current						
I_B	Input bias current	T_A = 25°C		30	100	pA
		T_A = -40°C to 125°C			20	nA
I_{OS}	Input offset current			8		pA
C_{LOAD}	Capacitive load drive			60		pF
Output type		Open-drain				

AC Electrical Characteristics

V_{CC} = 2.55 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Power	Min	Typ	Max	Unit
Audio switch							
t_{delay}	Audio switch turn-on delay time	DP_R = DN_L = 1 V, R_L = 32 Ω	V_{CC} = 3.3 V		20		μs
t_{rise}	Audio switch turn-on rising time (1)	DP_R = DN_L = 1 V, R_L = 32 Ω			40		μs
t_{OFF}	Audio switch turn-off time	DP_R = DN_L = 1 V, R_L = 32 Ω			2		μs
X_{TALK}	Cross talk (adjacent)	f = 1 kHz, R_L = 50 Ω, V_{SW} = 1 V_{RMS}			-90		dB
BW	−3 dB bandwidth	R_L = 50 Ω			800		MHz
O_{IRR}	Off isolation	f = 1 kHz, R_L = 50 Ω, C_L = 0 pF, V_{SW} = 1 V_{RMS}			-95		dB
THD+N	Total harmonic distortion + noise performance with A−weighting filter	R_L = 600 Ω, f = 20 Hz~20 kHz, V_{SW} = 2 V_{RMS}			-110		dB
		R_L = 32 Ω, f = 20 Hz~20 kHz, V_{SW} = 1 V_{RMS}			-110		dB

		R_L = 16 Ω, f = 20 Hz~20 kHz, V_{SW} = 0.5 V_{RMS}			-108		dB
USB switch							
t_{ON}	USB switch turn−on time	DP_R = DN_L = 1.5 V, R_L = 50 Ω	V_{CC} = 3.3 V		30		μs
t_{OFF}	USB switch turn−off time	DP_R = DN_L = 1.5 V, R_L = 50 Ω			3		μs
BW	−3 dB bandwidth	R_L = 50 Ω			950		MHz
O_{IRR}	Off isolation between DP, DN and common node pins	f = 1 kHz, R_L = 50 Ω, C_L = 0 pF, V_{SW} = 1 V_{RMS}			-100		dB
t_{OVP}	DP_R and DN_L pins OVP response time	V_{SW} = 3.5 V to 5.5 V			0.4		μs
UART switch							
BW	−3 dB bandwidth	R_L = 50 Ω	V_{CC} = 3.3 V		800		MHz
MIC/Audio ground switch							
t_{delay_MIC}	MIC switch turn-on delay time	SBUx = 1 V, R_L = 50 Ω	V_{CC} = 3.3 V		100		μs
t_{rise_MIC}	MIC switch turn-on rising time (1)				120		
t_{delay_AGND}	AGND switch turn-on time	SBUx pulled to 0.5 V by 16 Ω, AGND connect to GND			1		ms
t_{rise_AGND}	AGND switch turn-on rising time(1)				1.5		
t_{OFF_MIC}	MIC switch turn-off time	SBUx = 2.5 V, R_L = 50 Ω			1		μs
$t_{OFF\_Audio\ GND}$	AGND switch turn-off time	SBUx: Isource = 10 mA, clamp to 2.5 V			50		μs
BW	MIC switch bandwidth	R_L = 50 Ω			60		MHz
SBUx_H switch							
t_{ON}	SBUx_H switch turn-on time	SBUx = 2.5 V, R_L = 50 Ω	V_{CC} = 3.3 V		40		μs
t_{OFF}	SBUx_H switch turn-off time				1		μs
BW	Bandwidth	R_L = 50 Ω			60		MHz
t_{OVP}	SBUx pins OVP response time	V_{SW} = 3.5 V to 5.5 V			0.4		μs

Note:

(1) The turn-on timing can be controlled by the I^2C register.

(2) Specifications subject to change without notice.

I²C Specification

V_{CC} = 2.55 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	I²C_SCL clock frequency			400	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition	0.6			μs
t_{LOW}	Low period of I²C_SCL clock	1.3			μs
t_{HIGH}	High period of I²C_SCL clock	0.6			μs
$t_{SU;\ STA}$	Set−up time for repeated START condition	0.6			μs
$t_{HD;\ DAT}$	Data hold time (1)	0		0.9	μs
$t_{SU;\ DAT}$	Data set−up time (2)	100			ns
t_r	Rising time of I²C_SDA and I²C_SCL signals (2)	20 + 0.1 Cb		300	ns
t_f	Falling time of I²C_SDA and I²C_SCL signals (2)	20 + 0.1 Cb		300	ns
$t_{SU;\ STO}$	Set−up time for STOP condition	0.6			μs
t_{BUF}	Bus−free time between STOP and START conditions	1.3			μs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0		50	ns

Note:

(1) Guaranteed by characterization. Not production tested.

(2) A fast−mode I²C−bus device can be used in a standard−mode I²C−bus system, but the requirement $t_{SU;DAT}$ ≥ ±250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I²C_SCL signal. If such a device does stretch the LOW period of the I²C_SCL signal, it must output the next data bit to the I²C_SDA line t_{r_max} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the I²C_SCL line is released.

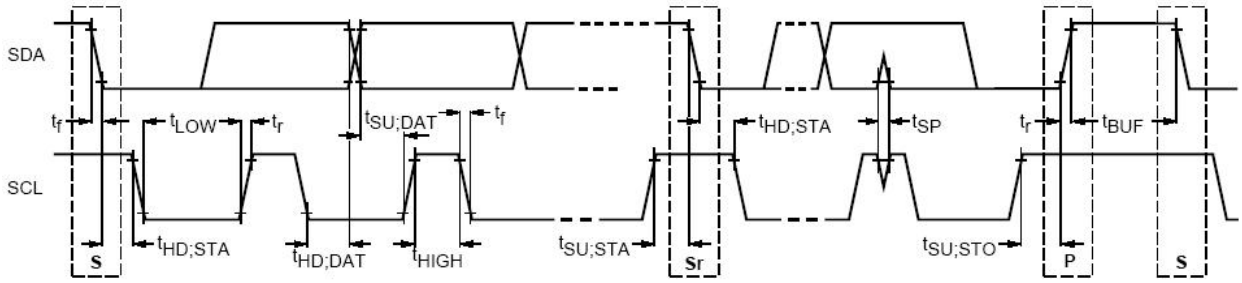


Figure 3. Definition of timing for full−speed mode devices on the I²C bus

Capacitance

V_{CC} = 2.55 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C.

Symbol	Parameter	Conditions	Power	Min	Typ	Max	Unit
$C_{ON\_USB/Audio}$	On capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias	V_{CC} = 3.3 V		8		pF
$C_{OFF\_USB/Audio}$	Off capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias			6.5		pF
C_{OFF_USB}	Off capacitance (non−common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias			2.6		pF
$C_{ON\_SENSE\_SW}$	On capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias			55		pF
$C_{OFF\_SENSE\_SW}$	Off capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias			88		pF
$C_{ON\_MIC\_SW}$	On capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias			170		pF
$C_{OFF\_MIC\_SW}$	Off capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias			10		pF
$C_{ON\_AGND\_SW}$	On capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100mV DC bias			125		pF
$C_{ON\_SBUx\_H\_SW}$	On capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias			160		pF

Note:

(1) Specifications subject to change without notice.

Register Maps

ADDR	Register Name	Type	Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	Device ID	R	0XF5	1	1	1	1	0	1	0	1
02H	OVP interrupt flag	R/C	0x00	Reserved	Reserved	OVP/ DP_R	OVP/ DN_L	OVP/ SBU1,SBU2		OVP/ GSBU1	OVP/ GSBU2
03H	OVP status	R	0x00	Reserved	Reserved	OVP/ DP_R	OVP/ DN_L	OVP/ SBU1,SBU2		OVP/ GSBU1	OVP/ GSBU2
04H	Switch settings enable	R/W	4483: 0xF8 4483B: 0x98	Device enable	SBU1_H to SBUx	SBU2_H to SBUx	DN_L to DN or L	DP_R to DP or R	Sense to GSBUx	MIC to SBUx	AGND to SBUx switches
05H	Switch select	R/W	0x18	USB2 switch select	SBU1_H switches	SBU2_H switches	DN_L to DN1 or L switches	DP_R to DP1 or R switches	Sense to GSBUx	MIC to SBUx	AGND to SBUx switches
06H	Switch status0	R	0x05	Reserved		Sense switch status		DP_R switch status		DN_L switch status	
07H	Switch status1	R	4483: 0x23 4483B: 0x00	Reserved		SBU2 switch status			SBU1 switch status		
08H	Audio switch left channel turn-on control	R/W	0x01	Audio switch left channel slow control [7:0]							
09H	Audio switch right channel turn-on control	R/W	0x01	Audio switch right channel slow control [7:0]							
0AH	MIC switch turn-on control	R/W	0x01	MIC switch slow control [7:0]							
0BH	Sense switch turn-on control	R/W	0x01	Sense switch slow control [7:0]							
0CH	Audio ground switch turn-on control	R/W	0x01	Audio ground switch slow control [7:0]							
0DH	Timing delay between R switch enable and switch on order	R/W	0x00	Timing delay between R switch enable and switch on order control [7:0]							
0EH	Timing delay between MIC switch enable and switch on order	R/W	0x00	Timing delay between MIC switch enable and switch on order control [7:0]							

0FH	Timing delay between Sense switch enable and switch on order	R/W	0x00	Timing delay between Sense switch enable and switch on order control [7:0]						
10H	Timing delay between Audio ground switch enable and switch on order	R/W	0x00	Timing delay between Audio ground switch enable and switch on order control [7:0]						
11H	Audio accessory status	R	0x01	Reserved					CC_IN	Reserved
12H	Function enable	R/W	0x00	OVP threshold voltage configuration	Reserved	GPIO control enable	Slow turn-on control enable	MIC auto break out control enable	Reserved	Audio jack detection and configuration enable
17H	Audio jack status	R	0x01	Reserved			4 pole, SBU2 to MIC	4 pole, SBU1 to MIC	3 pole	No audio
18H	Audio jack detection/ watchdog interrupt flag	R/C	0x00	Reserved			Watchdog timeout	Audio jack detection and Configura-tion	Reserved	
1CH	MIC detection threshold DATA0	R/W	0x20	MIC threshold value DATA0 [7:0]						
1DH	MIC detection threshold DATA1	R/W	0xFF	MIC threshold value DATA1 [7:0]						
1EH	I²C reset	W/C	0x00	Reserved						I²C reset
1FH	Current source setting	R/W	0x07	Reserved			Current source setting [3:0]			
20H	Watchdog setting	R/W	0x01	Watchdog enable	Reserved		Watchdog reset	Watchdog timer		
21H	Timing delay between L switch enable and switch on order	R/W	0x00	Timing delay between L switch enable and switch on order control [7:0]						

I²C Slave Address

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	0	0	0	1	0	R/W

Register Definition

Device ID

Address: 00h

Reset Value: 8'b 1111_0101

Type: Read

Bits	Name	Size	Description
7:6	Vendor ID	2	Vendor ID
5:3	Version ID	3	Device version ID
2:0	Revision ID	3	Revision history ID

OVP interrupt flag

Address: 02h

Reset Value: 8'b 0000_0000

Type: Read Clear

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
5	DP_R OVP	1	0: OVP event has not occurred 1: OVP event has occurred
4	DN_L OVP	1	0: OVP event has not occurred 1: OVP event has occurred
[3:2]	SBU1 || SBU2 OVP	2	0: OVP event has not occurred 1: At least one of SBU1 or SBU2 OVP event has occurred
1	GSBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
0	GSBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred

OVP status

Address: 03h

Reset Value: 8'b 0000_0000

Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use

5	OVP on DP_R PIN	1	0: OVP event has not occurred 1: OVP event has occurred
4	OVP on DN_L PIN	1	0: OVP event has not occurred 1: OVP event has occurred
[3:2]	SBU1 || SBU2 OVP	2	0: OVP event has not occurred 1: At least one of SBU1 or SBU2 OVP event has occurred
1	OVP on GSBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
0	OVP on GSBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred

Switching setting enable

Address: 04h

Reset Value: DIO4483: 8'b 1111_1000

DIO4483B: 8'b 1001_1000

Type: Read/Write

Bits	Name	Size	Description
7	Device enable	1	1: Device enable. 0: Device disable; L, R pull down by 10 kΩ and other switch nodes will be high−Z for positive input.
6	SBU1_H to SBUx switches	1	0: Switch disable; SBU1_H will be high−Z for positive input 1: Switch enable
5	SBU2_H to SBUx switches	1	0: Switch disable; SBU2_H will be high−Z for positive input 1: Switch enable
4	DN_L to DN1/2 or L switches	1	0: Switch disable; DN_L, DN1/2 will be high−Z for positive input. L pull down by 10 kΩ 1: Switch enable
3	DP_R to DP1/2 or R switches	1	0: Switch disable; DP_R, DP1/2 will be high−Z for positive input. R pull down by 10 kΩ 1: Switch enable
2	Sense to GSBUx switches	1	0: Switch disable; Sense, GSBU1 and GSBU2 will be high−Z for positive input 1: Switch enable
1	MIC to SBUx switches	1	0: Switch disable: MIC will be high−Z for positive input. 1: Switch enable
0	AGND to SBUx switches	1	0: Switch disable: AGND will be high−Z for positive input. 1: Switch enable

Switch select

Address: 05h

Reset Value: 8'b 0001_1000

Type: Read/Write

Bits	Name	Size	Description
7	USB2 switch select	1	0: USB2 off. USB1 or Audio switch depend on 05h, bit <4:3> and 04h,bit <4:3> 1: DP/R~DP2, DN/L~DN2 switches ON,if 04h, bit<4:3> = '11' and 05h, bit <4:3> = '11'
6	SBU1_H switches	1	0: SBU1_H to SBU1 switch ON 1: SBU1_H to SBU2 switch ON
5	SBU2_H switches	1	0: SBU2_H to SBU2 switch ON 1: SBU2_H to SBU1 switch ON
4	DN_L to DN1 or L switches	1	0: DN_L to L switch ON 1: DN_L to DN1 switch ON
3	DP_R to DP1 or R switches	1	0: DP_R to R switch ON 1: DP_R to DP1 switch ON
2	Sense to GSBUx switches	1	0: Sense to GSBU1 switch ON 1: Sense to GSBU2 switch ON
1	MIC to SBUx switches	1	0: MIC to SBU2 switch ON 1: MIC to SBU1 switch ON
0	AGND to SBUx switches	1	0: AGND to SBU1 switch ON 1: AGND to SBU2 switch ON

Note: If want to change to USB2 mode, you must first write 0x05h = 0x98h, then write 0x04h = 0x98h

Switch status0

Address: 06h

Reset Value: 8'b 0000_0101

Type: Read Only

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:4]	Sense switch status	2	00: Sense switch is Open/Not Connected 01: Sense connected to GSBU1 10: Sense connected to GSBU2 11: Not valid
[3:2]	DP_R switch status	2	00: DP_R Switch Open/Not Connected 01: DP_R connected to DP1 10: DP_R connected to R 11: DP_R connected to DP2
[1:0]	DN_L switch status	2	00: DN_L Switch Open/Not Connected 01: DN_L connected to DN1 10: DN_L connected to L 11: DN_L connected to DN2

Switch status1

Address: 07h

Reset Value: DIO4483: 8'b 0010_0011

DIO4483B: 8'b 0000_0000

Type: Read Only

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:3]	SBU2 switch status	3	000: SBU2 switch is Open/Not Connected 001: SBU2 connected to MIC 010: SBU2 connected to AGND 011: SBU2 connected to SBU1_H 100: SBU2 connected to SBU2_H 101: SBU2 connected both SBU1_H and SBU2_H 110…111: Do not use
[2:0]	SBU1 switch status	3	000: SBU1 switch is Open/Not Connected 001: SBU1 connected to MIC 010: SBU1 connected to AGND 011: SBU1 connected to SBU1_H 100: SBU1 connected to SBU2_H 101: SBU1 connected both SBU1_H and SBU2_H 110…111: Do not use

Audio switch left channel slow turn-on

Address: 08h

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111:25600 μs
			…
			00000001: 200 μs
			00000000: 100 μs

Audio switch right channel slow turn-on

Address: 09h

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25600 μs
			…
			00000001: 200 μs
			00000000: 100 μs

MIC switch slow turn-on

Address: 0Ah

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25700 μs
			…
			00000010: 350 μs
			00000001: 250 μs
			00000000: not valid

Sense switch slow turn-on

Address: 0Bh

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn-on rising time setting	8	11111111: 25600 μs
			…
			00000001: 200 μs
			00000000: 100 μs

Audio ground switch slow turn-on

Address: 0Ch

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn-on rising time setting	8	11111111: 179000 μs
			…
			00000001: 1400 μs
			00000000: 700 μs

Timing delay between R switch enable and switch on order

Address: 0Dh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 ms

			…
			00000001: 400 μs
			00000000: 0 μs

Timing delay between MIC switch enable and switch on order

Address: 0Eh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 μs
			…
			00000001: 400 μs
			00000000: 0 μs

Timing delay between Sense switch enable and switch on order

Address: 0Fh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110:101.6 ms
			…
			00000001: 400 μs
			00000000: 0 μs

Timing Delay between Audio ground switch enable and switch on order

Address: 10h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 ms
			…
			00000001: 400 μs
			00000000: 0 μs

Audio accessory status

Address: 11h

Reset Value: 8'b 0000_0001

Type: Read

Bits	Name	Size	Description
[7:2]	Reserved	6	Do not use
1	CC_IN	1	0: CC_IN < 1.2 V 1: CC_IN > 1.5 V
0	Reserved	1	Do not use

Function enable

Address: 12h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:6]	OVP threshold voltage configuration	2	00: 4.4 V 01: 4.6 V 10: 4.8 V 11: 5.0 V
5	Reserved	1	Do not use
4	GPIO control enable	1	Do not use
3	Slow turn on control enable	1	1: Enable 0: Disable
2	MIC auto break out control enable	1	1: Enable 0: Disable
1	Reserved	1	Do not use
0	Audio jack detection and configuration enable	1	1: Enable; will be changed to '0' after audio jack detection and configuration 0: Disable

Audio jack status

Address: 17h

Reset Value: 8'b 0000_0001

Type: Read

Bits	Name	Size	Description
[7:4]	Reserved	4	Do not use
3	4 pole	1	1: 4 Pole SBU2 to MIC, SBU1 to audio ground 0: others
2	4 pole	1	1: 4 Pole SBU1 to MIC, SBU2 to audio ground 0: others
1	3 pole	1	1: 3 pole 0: others

0	No audio accessory	1	1: No audio accessory 0: Audio accessory attached

Audio jack detection/watchdog interrupt flag

Address: 18h

Reset Value: 8'b 0000_0000

Type: Read Clear

Bits	Name	Size	Description
[7:4]	Reserved	4	Do not use
3	Watchdog timeout	1	0: Watchdog timeout has not occurred 1: Watchdog timeout has occurred
2	Audio jack detection and configuration	1	0: Audio jack detection and configuration has not occurred 1: Audio jack detection and configuration has occurred
[1:0]	Reserved	2	Do not use

MIC detection threshold data0

Address: 1Ch

Reset Value: 8'b 0010_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA0	8	MIC detection threshold DATA0 0010_0000: 300 mV

MIC detection threshold data1

Address: 1Dh

Reset Value: 8'b 1111_1111

Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold DATA1	8	MIC detection threshold DATA1 1111_1111: 2.4 V

I^2C reset

Address: 1Eh

Reset Value: 8'b 0000_0000

Type: W/C

Bits	Name	Size	Description
[7:1]	Reserved	7	Reserved
0	I^2C reset	1	0: default 1: I^2C reset

Current source setting

Address: 1Fh

Reset Value: 8'b 0000_0111

Type: Read/Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Reserved
[3:0]	Current source setting	4	1111: 1500 μA 0111: 700 μA 0001: 100 μA 0000: Invalid

Watchdog setting

Address: 20h

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
7	Watchdog enable	1	0: Watchdog disabled 1: Watchdog enabled
[6:4]	Reserved	3	Reserved
3	Watchdog reset	1	
[2:0]	Watchdog timer	3	000: 0.5 s 001: 1 s 010: 2 s 011: 5 s 100: 10 s 101: 30 s 110: 60 s 111: 5 min

Note: When WD is enabled, if watchdog reset (20h, bit <3>) = 0, IC will reset to USB1 state per 1 s (configured by bit <2:0>).

Timing delay between L switch enable and switch on order

Address: 21h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 ms
			…
			00000001: 400 μs
			00000000: 0 μs

Application Information

Over-Voltage Protection

The DIO4483/4483B features an over−voltage protection (OVP) on receptacle side pins that turns off the internal signal routing path if the voltage exceeds the OVP threshold. If an OVP is occurred, flag register 0x02h and 0x03h will indicate which pin had the OVP event. OVP threshold voltage is configurable by 0x12h, bit [7:6].

Headset Detection

The DIO4483/4483B integrates headset unplug detection function by detecting the CC_IN voltage. The function will be active when device is enabled. Register 0x11h, bit[1:0] Output can indicate if CC_IN is low (CC_IN < 1.2 V) or high (CC_IN > 1.5 V).

	0x11h, bit [1]	0x11h, bit [0]
CC_IN < 1.2 V	0	1
CC_IN > 1.5 V	1	0

MIC Switch Auto−off Function

The function is active during control bit 0x12h bit [2] = 1. When CC_IN is changed from low to high, and L, R, and AGND switches are on, the MIC switch will be off and receptacle side pin will be pulled to ground for 50 μs first. Then it shows high−Z status under MIC switch is set on status.

Audio Jack Detection and Configuration

The function is active when control bit 0x12h bit [0] = 1. When the headset is inserted, the DIO4483/4483B can detect OMTP, CTIA or 3-Pole headset and configurate pinout automatically. During detection and configuration, the R, L, Sense, MIC and Audio ground switches will be off. After detection and configuration, R, L, MIC, Sense and AGND switches will turn on according to detection results and timing control setting.

I²C Interface

The DIO4483/4483B includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz, signals. Examples of an I²C write and read sequence are shown in below figures respectively.

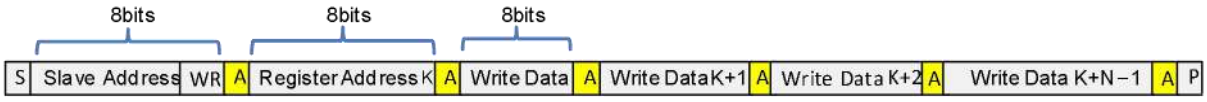


Figure 4. I²C Write Example

Note: Single-byte read is initiated by the master with P immediately following the first data byte.

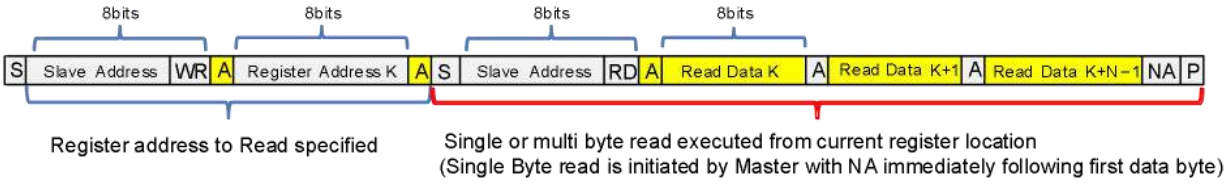


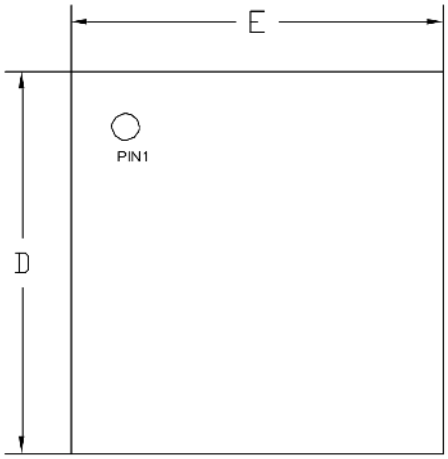
Figure 5. I²C read example

Note: If the register is not specified, the master will begin reading from the current register. In this case only sequence showing in the red bracket is needed

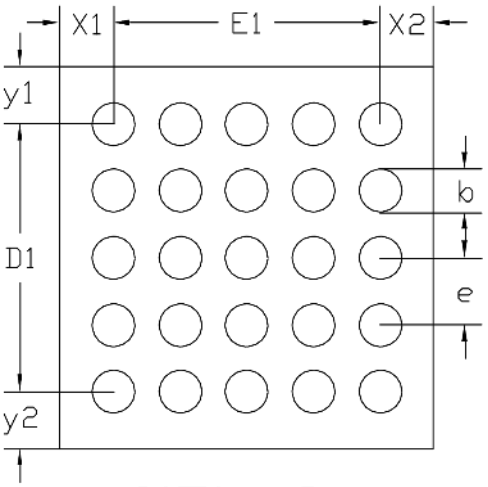
From Master to Slave
From Slave to Master

S Start Condition
A Acknowledge (SDA Low)
NA NOT Acknowledge (SDA High)
WR Write= 0
RD Read =1
P Stop Condition

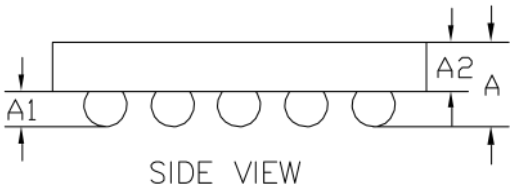
Physical Dimensions: WLCSP-25



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.541	0.586	0.631
A1	0.190	0.210	0.230
A2	0.351	0.376	0.401
D	2.250	2.280	2.310
D1		1.600 BSC	
E	2.210	2.240	2.270
E1		1.600 BSC	
b	0.238	0.258	0.278
e		0.400 BSC	
x1		0.320 REF	
x2		0.320 REF	
y1		0.340 REF	
y2		0.340 REF	

CONTACT US

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