# 8-BIT SHIFT REGISTER WITH 8-BIT OUTPUT REGISTER

## Description

The 74HCT595 is an high speed CMOS device that is designed to be pin compatable with 74LS low power Schottky types.

An eight bit shift register accpets data from the serial input (DS) on each positive transition of the shift register clock (STCP). When asserted low the reset function ($\overline{MR}$) sets all shift register values to zero and is indepent of all clocks.

Data from the input serial shift register is placed in the output register with a rising pulse on the storages resister clock (SHCP). With the output enable ($\overline{OE}$) asserted low the 3-state outputs Q0-Q7 become active and present th

All registers capture data on rising edge and change output on the falling edge. If both clocks are connected together the input shift register is always one clock cycle ahead of the output register.
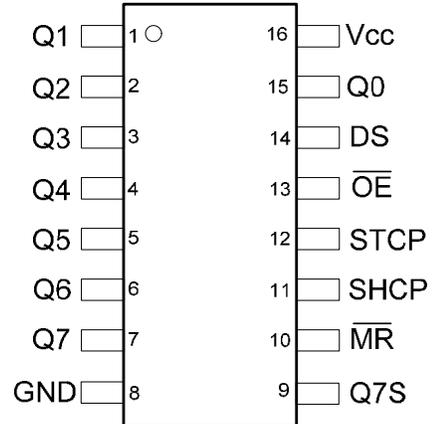
## Pin Assignments

( Top View )

| Q1 | 1 ○ | 16 | Vcc |
| Q2 | 2 | 15 | Q0 |
| Q3 | 3 | 14 | DS |
| Q4 | 4 | 13 | $\overline{OE}$ |
| Q5 | 5 | 12 | STCP |
| Q6 | 6 | 11 | SHCP |
| Q7 | 7 | 10 | $\overline{MR}$ |
| GND | 8 | 9 | Q7S |

**SO-16 / TSSOP-16**

## Features

- Supply Voltage Range from 4.5V to 5.5V
- Sinks or sources 8mA at $V_{CC}$ = 4.5V
- CMOS low power consumption
- Schmitt Trigger Action at All Inputs
- Inputs accept up to 6.0V
- ESD Protection Tested per JESD 22
  - Exceeds 200-V Machine Model (A115-A)
  - Exceeds 2000-V Human Body Model (A114-A)
  - Exceeds 1000-V Charged Device Model (C101C)
- Latch-Up Exceeds 250mA per JESD 78, Class II
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
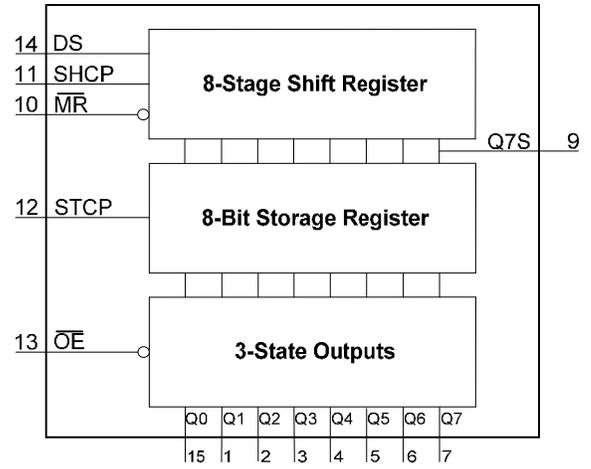
## Applications

- General Purpose Logic
- Serial to Parallel Data conversion
- Capture and hold data for extended periods of time.
- Allow simple serial bit streams from a microcontroller to control as many peripheral lines as needed.
- Wide array of products such as:
  - Computer peripherals
  - Appliances
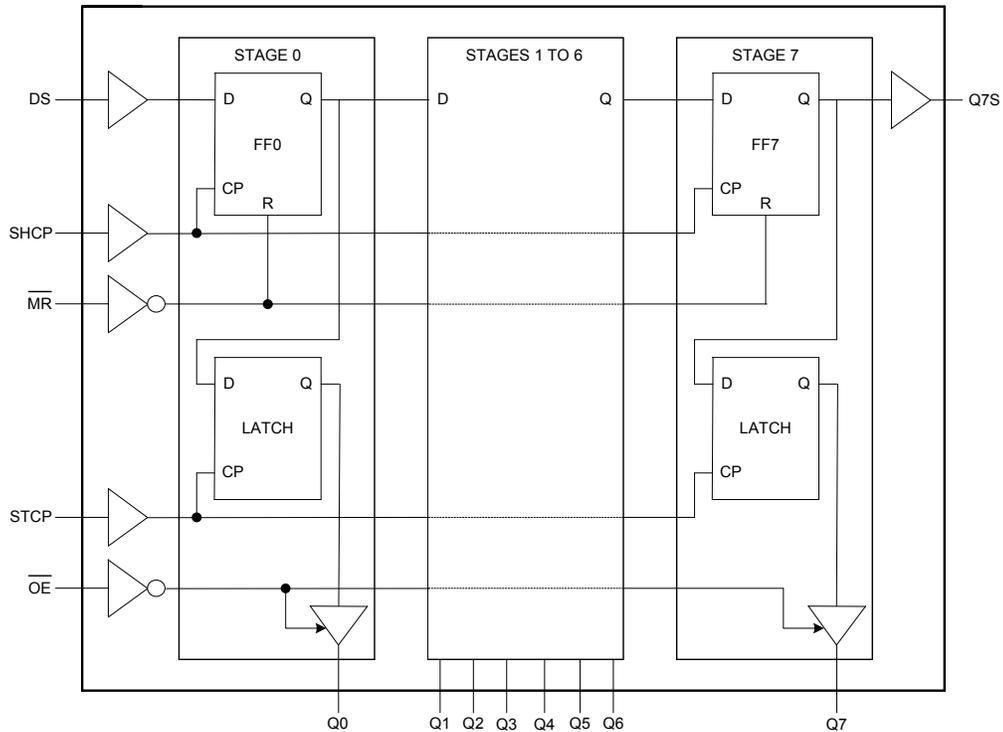  - Industrial control

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74HCT595
Document number: DS35493 Rev. 3 - 2

1 of 11
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## Pin Descriptions

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | Q1 | Parallel Data Output 1 |
| 2 | Q2 | Parallel Data Output 2 |
| 3 | Q3 | Parallel Data Output 3 |
| 4 | Q4 | Parallel Data Output 4 |
| 5 | Q5 | Parallel Data Output 5 |
| 6 | Q6 | Parallel Data Output 6 |
| 7 | Q7 | Parallel Data Output 7 |
| 8 | GND | Ground |
| 9 | Q7S | Serial Data Output |
| 10 | $\overline{MR}$ | Master Reset Input |
| 11 | SHCP | Shift Register Clock Input |
| 12 | STCP | Storage Register Clock Input |
| 13 | $\overline{OE}$ | Output Enable Input |
| 14 | DS | Serial Data Input |
| 15 | Q0 | Parallel Data Output 0 |
| 16 | Vcc | Supply Voltage |

## Functional Diagram



## Logic Diagram

74HCT595
Document number: DS35493 Rev. 3 - 2

2 of 11
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## Functional Description and Timing Diagram

| Control | | | | Input | Output | | Function |
|---|---|---|---|---|---|---|---|
| SHCP | STCP | $\overline{OE}$ | $\overline{MR}$ | DS | Q7S | Qn | |
| X | X | L | L | – | L | NC | Low-level asserted on MR clears shift register<br>Storage register is unchanged |
| X | ↑ | L | L | – | L | L | Empty shift register transferred to storage register |
| X | X | H | L | – | L | Z | Shift register remains clear; All Q ouputs in Z state |
| ↑ | X | L | H | – | Q6S | NC | HIGH is shifted into first stage of Shift Register Contents of each register shifted to next register<br>The content of Q6S has been shifted to Q7S and now appears on device pin Q7S |
| X | ↑ | L | H | – | NC | QnS | Contents of shift register copied to storage register<br> With output now in active state, the storage resister contents appear on Q outputs |
| ↑ | ↑ | L | H | – | Q6S | QnS | Contents of shift register copied to output register then shift register shifted. |

H=HIGH voltage state
L=LOW voltage state
↑=LOW to HIGH transition
X= don't care – high or low (not floating)
NC= No change
Z= high-impedance state



74HCT595
Document number: DS35493 Rev. 3 - 2

3 of 11
**www.diodes.com**

July 2013
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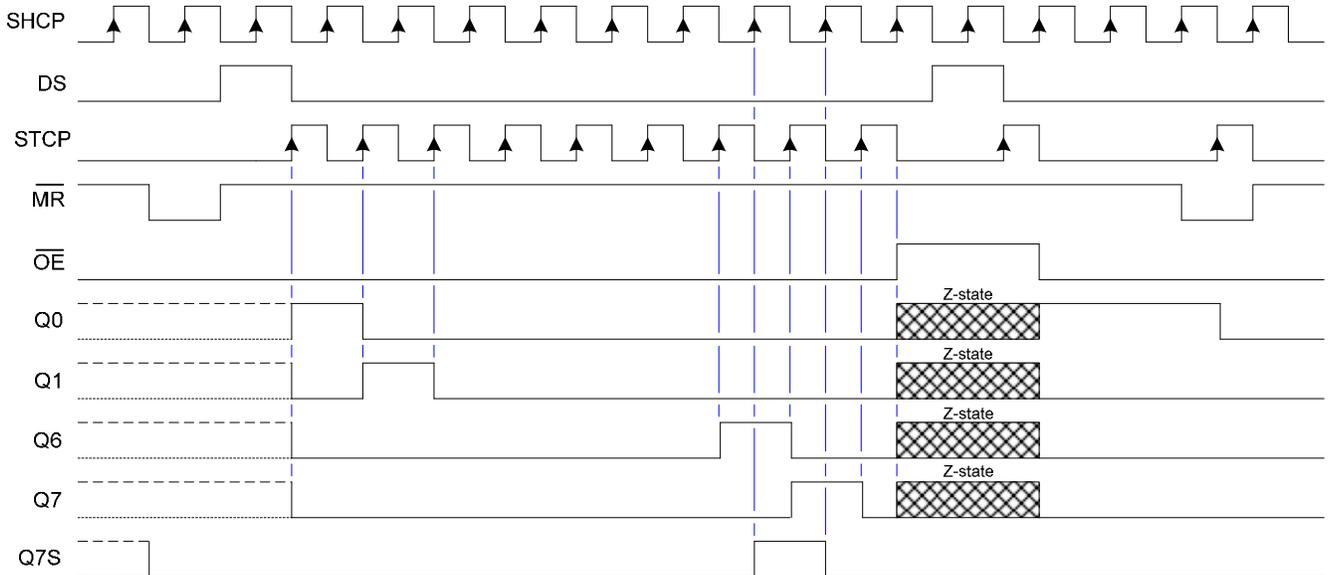
## Absolute Maximum Ratings (Note 4) (@T$_A$ = +25°C°C, unless otherwise specified.)

| Symbol | Description | | Rating | Unit |
|---|---|---|---|---|
| ESD HBM | Human Body Model ESD Protection | | 2 | kV |
| ESD CDM | Charged Device Model ESD Protection | | 1 | kV |
| ESD MM | Machine Model ESD Protection | | 200 | V |
| V$_{CC}$ | Supply Voltage Range | | -0.5 to +7.0 | V |
| V$_I$ | Input Voltage Range | | -0.5 to +7.0 | V |
| V$_o$ | Voltage applied to output in high or low state | | -0.3 to V$_{CC}$ +0.5 | V |
| I$_{IK}$ | Input Clamp Current   V$_I$ < -0.5V | | -20 | mA |
| I$_{IK}$ | Input Clamp Current   V$_I$ > Vcc +0.5V | | 20 | mA |
| I$_{OK}$ | Output Clamp Current   V$_O$ < -0.5V | | -20 | mA |
| I$_{OK}$ | Output Clamp Current   V$_O$ > V$_{CC}$ + 0.5V | | 20 | mA |
| I$_O$ | Continuous output current | Q7 standard output | +/- 25 | mA |
| | | Qn bus driver outputs | +/- 35 | mA |
| I$_{CC}$ | Continuous current through V$_{CC}$ or GND | | 70 | mA |
| I$_{GND}$ | Continuous current through V$_{CC}$ or GND | | -70 | mA |
| T$_J$ | Operating Junction Temperature | | -40 to +150 | °C |
| T$_{STG}$ | Storage Temperature | | -65 to +150 | °C |
| P$_{TOT}$ | Total Power Dissipation | | 500 | mW |

Note:    4. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values, and device operation should be within recommend values.

## Recommended Operating Conditions (Note 5)  (@T$_A$ = +25°C°C, unless otherwise specified.)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| V$_{CC}$ | Supply Voltage | – | 4.5 | 5.5 | V |
| V$_I$ | Input Voltage | – | 0 | 5.5 | V |
| V$_O$ | Output Voltage | Active Mode | 0 | V$_{CC}$ | V |
| Δt/ΔV | Input transition rise or fall rate | V$_{CC}$ = 4.5V to  5.5V | – | 100 | ns/V |
| T$_A$ | Operating free-air temperature | – | -40 | 125 | °C |

Note:   5. Unused inputs should be held at V$_{cc}$ or Ground.

74HCT595
Document number: DS35493 Rev. 3 - 2

4 of 11
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## Electrical Characteristics (@T$_A$ = +25°C°C, unless otherwise specified.)

| Symbol | Parameter | Test Conditions | V$_{CC}$ | T$_A$ = +25°C°C | | | T$_A$ = -40°C°C to +85°C°C | | T$_A$ = -40°C°C to +125°C°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V$_{IH}$ | High-Level Input Voltage | – | 4.5V to 5.5V | 2.0 | – | – | 2.0 | – | 2.0 | – | V |
| V$_{IL}$ | Low-Level Input Voltage | – | 4.5V to 5.5V | – | – | 0.8 | – | 0.8 | – | 0.8 | V |
| V$_{OH}$ | High-Level Output Voltage | I$_{OH}$ = -20µA All outputs | 4.5V | 4.4 | 4.5 | – | 4.4 | – | 4.4 | – | V |
| | Q7S output | I$_{OH}$ = -4mA | 4.5V | 3.84 | 4.32 | – | 4.32 | – | 3.7 | – | |
| | Qn Bus Outputs | I$_{OH}$ = -6.0mA | 4.5V | 3.7 | 4.32 | – | 4.32 | – | 3.7 | – | |
| V$_{OL}$ | Low-Level Output Voltage | I$_{OL}$ = 20µA All outputs | 4.5V | – | 0 | 0.1 | – | 0.1 | – | 0.1 | V |
| | Q7S output | I$_{OL}$ = 4mA | 4.5V | – | 0.15 | 0.33 | – | 0.33 | – | 0.4 | |
| | Qn Bus Outputs | I$_{OL}$ = 6.0mA | 4.5V | – | .016 | 0.33 | – | 0.33 | – | 0.4 | |
| I$_I$ | Input Current | V$_I$ =GND to 5.5V | 5.5V | – | – | ±0.1 | – | ± 1 | – | ± 1 | µA |
| I$_{OZ}$ | OFF-state output current | Qn internal high or low. V$_o$=Vcc or Gnd | 5.5V | – | – | ± 5 | – | ± 5 | – | ± 10 | µA |
| I$_{CC}$ | Supply Current | V$_I$ = GND or V$_{CC}$ I$_O$=0 | 5.5V | – | – | 8.0 | – | 80 | – | 160 | µA |
| ΔI$_{CC}$ | Additional Supply Current per Input | V$_I$ = V$_{CC}$ -2.1V I$_O$=0 | 4.5V to 5.5V | – | 100 | 450 | – | 450 | – | 490 | µA |
| C$_i$ | Input Capacitance | V$_i$ = V$_{CC}$ or GND | 5.5V | – | 4 | 10 | – | 10 | – | 10 | pF |

## Operating Characteristics (@T$_A$ = +25°C°C, unless otherwise specified.)

| Parameter | | Test Conditions | V$_{CC}$ = 5V | Unit |
|---|---|---|---|---|
| | | | TYP | |
| C$_{pd}$ | Power dissipation capacitance | f = 1 MHz all outputs switching-no load | 42 | pF |

74HCT595
Document number: DS35493 Rev. 3 - 2

5 of 11
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## Switching Characteristics

| Symbol / Parameter | Pins | Test Conditions | V$_{CC}$ | T$_A$ = +25°C°C | | | -40°C°C to +85°C°C | | -40°C°C to +125°C°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ. | Max | Min | Max | Min | Max | |
| f$_{MAX}$ Maximum Frequency | SHCP or STCP | Figure 1 | 4.5V to 5.5V | 30 | 52 | – | 24 | – | 20 | – | MHz |
| t$_W$ Pulse Width | SHCP HIGH or LOW | Figure 1 | 4.5V to 5.5V | 16 | 6 | – | 20 | – | 24 | – | ns |
| | STCP HIGH or LOW | Figure 1 | 4.5V to 5.5V | 16 | 5 | – | 20 | – | 24 | – | |
| | $\overline{MR}$ LOW | Figure 1 | 4.5V to 5.5V | 20 | 8 | – | 25 | – | 30 | – | |
| t$_{SU}$ Set-up Time | DS to SHCP | Figure 1 | 4.5V to 5.5V | 16 | 5 | – | 20 | – | 24 | – | ns |
| | SHCP to STCP | Figure 1 | 4.5V to 5.5V | 16 | 8 | – | 20 | – | 24 | – | ns |
| t$_H$ Hold Time | DS to SHCP | Figure 1 | 4.5V to 5.5V | 3 | -2 | – | 3 | – | 3 | – | ns |
| t$_{REC}$ Recovery Time | $\overline{MR}$ to SHCP | Figure 1 | 4.5V to 5.5V | 10 | -7 | – | 13 | – | 15 | – | ns |
| t$_{PD}$ Propagation Delay | SHCP to Q7S | Figure 1 C$_L$=50pF | 4.5V to 5.5V | – | 25 | 42 | – | 53 | – | 63 | ns |
| | STCP to Qn | Figure 1 C$_L$=50pF | 4.5V to 5.5V | – | 24 | 40 | – | 50 | – | 60 | ns |
| | $\overline{MR}$ to Q7S | Figure 1 C$_L$=50pF | 4.5V to 5.5V | – | 23 | 40 | – | 50 | – | 60 | ns |
| t$_{EN}$ Enable Time | $\overline{OE}$ to Qn | Figure 1 C$_L$=50pF | 4.5V to 5.5V | – | 21 | 35 | – | 44 | – | 53 | ns |
| t$_{DIS}$ Disable Time | $\overline{OE}$ to Qn | Figure 1 C$_L$=50pF | 4.5V to 5.5V | – | 18 | 30 | – | 38 | – | 45 | ns |

74HCT595
Document number: DS35493 Rev. 3 - 2

6 of 11
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## Parameter Measurement Information
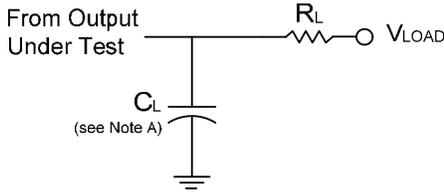


| TEST | Vload |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

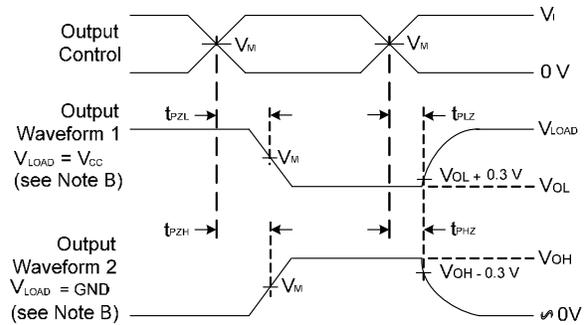| $V_{CC}$ | Inputs | | $V_M$ | | $C_L$ |
|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | Input | Output | |
| 4.5V to 5.5V | 3.0V | 3ns | 1.5V | $V_{CC}/2$ | 15pF, 50pF |
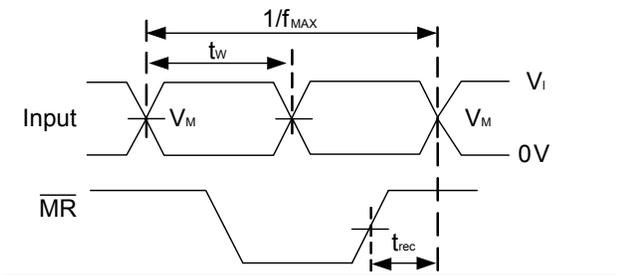


**Voltage Waveform**
**Pulse Duration and Recovery Time**
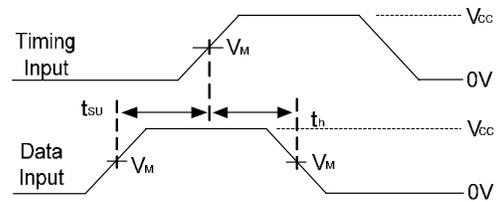
**Voltage Waveform**
**Set-up and Hold Times**
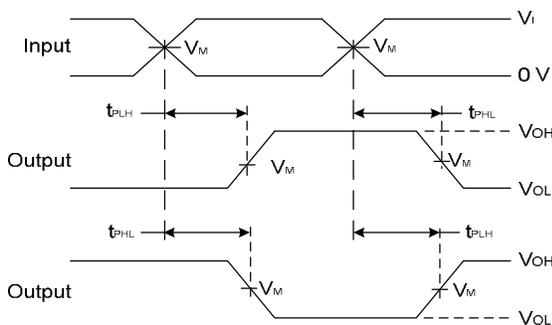
**Voltage Waveform**
**Propagation Delay Times**
**Inverting and Non Inverting Outputs**

**Voltage Waveform**
**Enable and Disable Times**

Notes: A . Includes test lead and test apparatus capacitance.
B. Output Waveform 1 depends on the internal $Q_N$ node being low and behaves in this manner based on OE pin.
Output Waveform 2 depends on the internal $Q_N$ node being high and behaves in this manner based on OE pin.
C. All pulses are supplied at pulse repetition rate ≤ 10 MHz
D. Inputs are measured separately one transition per measurement
E. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{PD}$

**Figure 1.  Load Circuit and Voltage Waveforms**

74HCT595
Document number: DS35493 Rev. 3 - 2

7 of 11
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## Ordering Information

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74  HCT 595  XXX - 13
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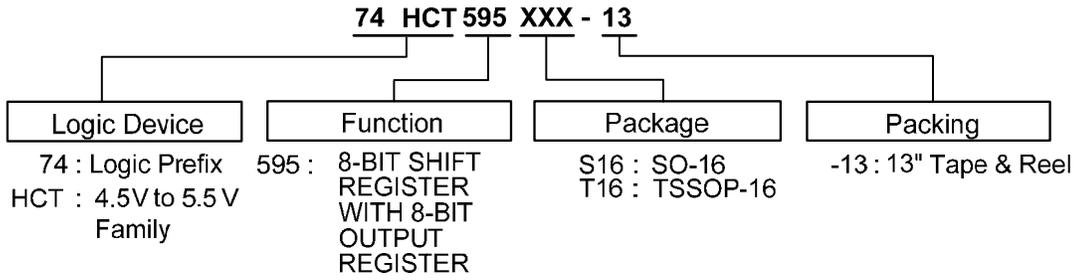
| Logic Device | Function | Package | Packing |
|---|---|---|---|
| 74 : Logic Prefix<br>HCT : 4.5V to 5.5 V Family | 595 : 8-BIT SHIFT REGISTER WITH 8-BIT OUTPUT REGISTER | S16 : SO-16<br>T16 : TSSOP-16 | -13 : 13" Tape & Reel |

| Device | Package Code | Packaging | 7" Tape and Reel(Note 6) | |
|---|---|---|---|---|
| | | | Quantity | Part Number Suffix |
| 74HCT595S16-13 | S16 | SO-16 | 2500/Tape & Reel | -13 |
| 74HCT595T16-13 | T16 | TSSOP-16 | 2500/Tape & Reel | -13 |

Notes:     6. . The taping orientation is located on our website at http://www.diodes.com/datasheets/ap02007.pdf

## Marking Information

**(1) SO-16, TSSOP-16**

( Top View )

Logo

Part Number

DII
**74HCT595**
YY WW X X

YY : Year : 08, 09,10~
WW : Week : 01~52; 52
represents 52 and 53 week
XX : Internal Codes
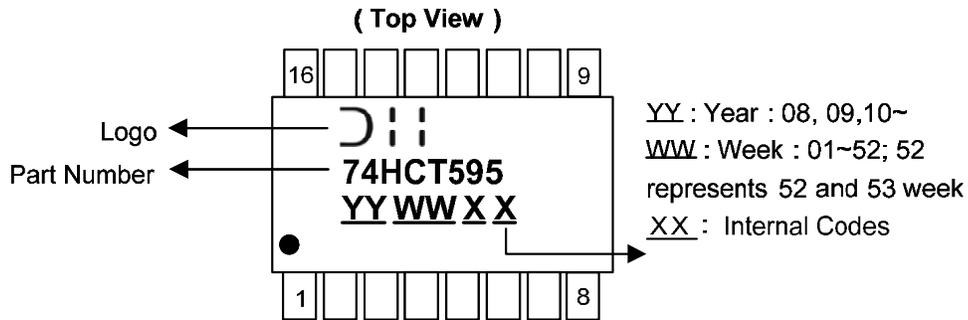
| Part Number | Package |
|---|---|
| 74HCT595S16 | SO-16 |
| 74HCT595T16 | TSSOP-16 |

74HCT595
Document number: DS35493 Rev. 3 - 2

8 of 11
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## Package Outline Dimensions (All Dimensions in mm)

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.

### (1)     Package Type: SO-16



| SO-16 | | |
|---|---|---|
| **Dim** | **Min** | **Max** |
| **A** | 1.40 | 1.75 |
| **A1** | 0.10 | 0.25 |
| **A2** | 1.30 | 1.50 |
| **B** | 0.33 | 0.51 |
| **C** | 0.19 | 0.25 |
| **D** | 9.80 | 10.00 |
| **E** | 3.80 | 4.00 |
| **e** | 1.27 Typ | |
| **H** | 5.80 | 6.20 |
| **L** | 0.38 | 1.27 |
| **Θ** | 0° | 8° |
| **All Dimensions in mm** | | |

### (2)     Package Type: TSSOP-16



Ø0.760Depth0.050±0.02

| TSSOP-16 | | | |
|---|---|---|---|
| **Dim** | **Min** | **Max** | **Typ** |
| **A** | - | 1.08 | - |
| **A1** | 0.05 | 0.15 | - |
| **A2** | 0.80 | 0.93 | - |
| **b** | 0.19 | 0.30 | - |
| **c** | 0.09 | 0.20 | - |
| **D** | 4.90 | 5.10 | - |
| **E** | 6.40 BSC | | |
| **E1** | 4.30 | 4.50 | - |
| **e** | 0.65 BSC | | |
| **L** | 0.45 | 0.75 | - |
| **L1** | 1.00  REF | | |
| **L2** | 0.25 BSC | | |
| **R** | 0.09 | - | - |
| **R1** | 0.09 | - | - |
| **X** | - | - | 1.350 |
| **Y** | - | - | 1.050 |
| **Θ** | 0° | 8° | - |
| **Θ1** | 5° | 15° | - |
| **Θ2** | 0° | - | - |
| **All Dimensions in mm** | | | |

74HCT595
Document number: DS35493 Rev. 3 - 2

9 of 11
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## Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

**Package Type: SO-16**
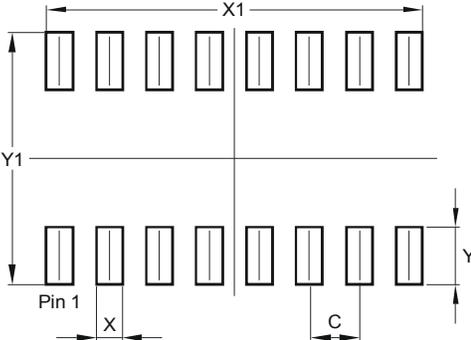
| Dimensions | Value (in mm) |
|---|---|
| **C** | 1.270 |
| **X** | 0.670 |
| **X1** | 9.560 |
| **Y** | 1.450 |
| **Y1** | 6.400 |

**Package Type: TSSOP-16**
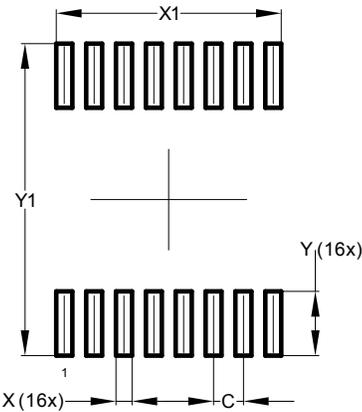
| Dimensions | Value (in mm) |
|---|---|
| **C** | 0.650 |
| **X** | 0.350 |
| **X1** | 4.900 |
| **Y** | 1.400 |
| **Y1** | 6.800 |

74HCT595
Document number: DS35493 Rev. 3 - 2

10 of 11
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**LIFE SUPPORT**

74HCT595
Document number: DS35493 Rev. 3 - 2

11 of 11
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