4-Channel EML Monitor and Controller with Positive/Negative Voltage and Current DAC

Features

- 4-Channel 12-Bit Voltage Output DAC
  - Positive and Negative Output Range: −5 V, −2.5 V, 2.5 V, 5 V
  - High Output Capability: 60 mA
- 4-Channel 12-Bit Current Output DAC
  - 200-mA Output Range
- 12-Bit ADC
  - 4 External Inputs
  - VDAC Current Monitor
- Internal Reference
  - 2.5 V
- Serial Interfaces
  - 4 Wire SPI
  - I^2C with 4 Slave Addresses
- Temperature Range: −40°C to +125°C
- Package: Wafer-Level CSP

Applications

- High-Speed Optical Module

Description

The TPAFEA008 is an integrated product with 4-ch negative/positive output VDAC and 4-ch IDAC, which is optimized for the optical module with 4-channel EML (Electro-absorption Modulated Laser).

The VDAC in TPAFEA008 supports both negative and positive output ranges, and the current capability is large enough to bias EAM (Electro-Absorption Modulator).

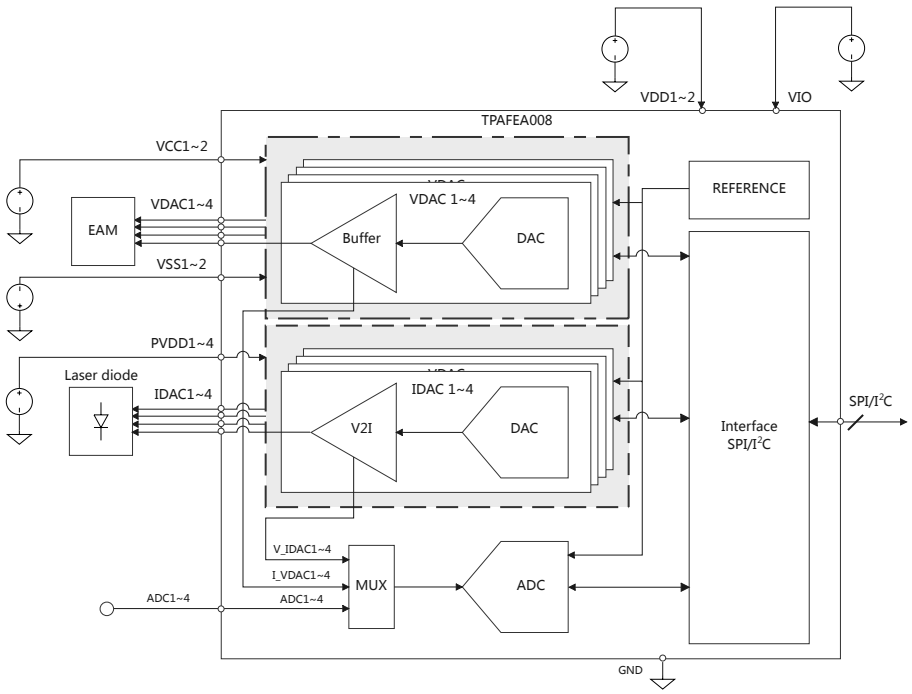
The IDAC in TPAFEA008 can support large output current range, and the output voltage range is also large enough to support different laser diodes.

The TPAFEA008 includes a 12bit ADC, with 4 input pins. Also, it incorporates internal alarm functions for ADC, so it can be used for RSSI (Received Signal Strength Indicator) and LOS (Loss of Signal) detection.

The VDAC output current and IDAC output voltage can be monitored by an integrated 12-bit ADC, so it is convenient for customers to monitor the loading status, without external components.

The TPAFEA008 is featured with small size, high integration, wide supply range, and operating temperature range, which make the device an excellent choice for 4-ch EML optical modules.

Typical Application Circuit



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Product Family Table

Order Number	VDAC Channel	IDAC Channel	ADC Channel	Package
TPAFEA008-WLPR	4	4	4	WLCSP

Revision History

Date	Revision	Notes
2023-06-05	Rev.A.0	Released version.
2023-08-18	Rev.A.1	Updated the output compliance voltage range and application information, and corrected unit typo.
2024-07-12	Rev.A.2	Updated the minimum operating voltage of VDAC.

Pin Configuration and Functions

TPAFEA008
WLCSP Package
Top View

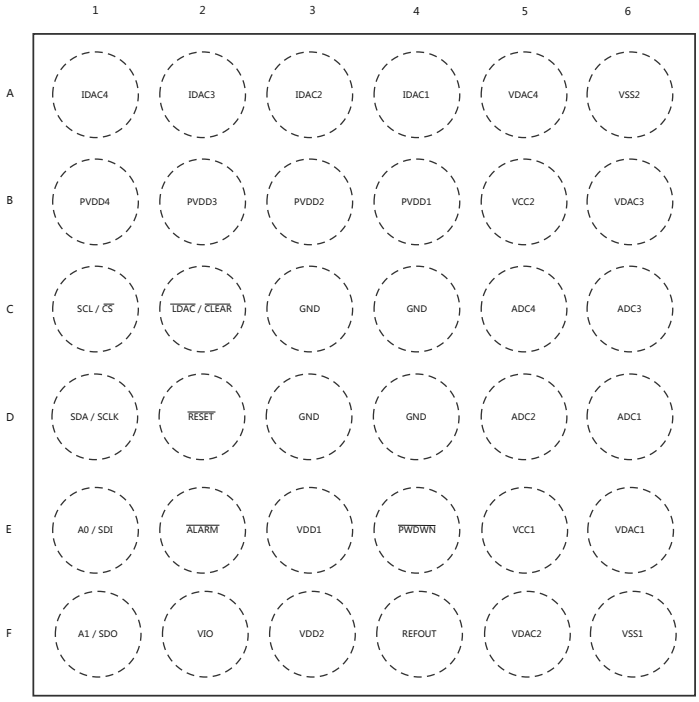

Table 1. Pin Functions: TPAFEA008

Pin		I/O	Description
No.	Name		
A1	IDAC4	Output	IDAC4 output.
A2	IDAC3	Output	IDAC3 output.
A3	IDAC2	Output	IDAC2 output.
A4	IDAC1	Output	IDAC1 output.
A5	VDAC4	Output	VDAC4 output.
A6	VSS2	Power	VDAC3~4 output buffers negative analog power supply. Must be tied to the same potential as VSS1.
B1	PVDD4	Power	IDAC4 output buffer analog power supply.
B2	PVDD3	Power	IDAC3 output buffer analog power supply.
B3	PVDD2	Power	IDAC2 output buffer analog power supply.
B4	PVDD1	Power	IDAC1 output buffer analog power supply.
B5	VCC2	Power	VDAC3~4 output buffers positive analog power supply. This pin must be tied to the same potential as VCC1.

Pin		I/O	Description
No.	Name		
B6	VDAC3	Output	VDAC3 output.
C1	SCL/ CS	Input	I^2C: Clock input.
			SPI: Active-low serial data enable. This input is the frame synchronization signal for the serial data. When the signal goes low, this pin enables the serial interface input shift register.
C2	LDAC/ CLR	Input	Active-low DAC synchronization signal. A high-to-low transition on the LDAC pin simultaneously updates the outputs of the IDACs and VDACs that are configured in synchronous mode. Alternatively, this pin can be configured as an active-low DAC clear signal to load the clear code for the IDACs or VDACs configured for a clear control.
C3	GND	Ground	Ground reference point for all circuitry on the device.
C4	GND	Ground	Ground reference point for all circuitry on the device.
C5	ADC4	Input	ADC4 analog input.
C6	ADC3	Input	ADC3 analog input.
D1	SDA/SCLK	Input/Output	I2C: Bidirectional data line. SPI: Clock input.
D2	RESET	Input	Active low reset input. Logic low on this pin initiates a reset event.
D3	GND	Ground	Ground reference point for all circuitry on the device.
D4	GND	Ground	Ground reference point for all circuitry on the device.
D5	ADC2	Input	ADC2 analog input.
D6	ADC1	Input	ADC1 analog input.
E1	A0/SDI	Input	I^2C: Slave address selector. SPI: Data input.
			Data are clocked into the input shift register on each falling edge of the SCLK pin.
E2	ALARM	Output	Alarm output. This pin is an open-drain, active-low output by default but can also be configured as a push-pull output or as an active-high output.
E3	VDD1	Power	Analog supply voltage. This pin must be tied to the same potential as VDD2. And it should be powered up before VCC1/2 or PVDD1/2/3/4.
E4	PWDWN	Input	Active low DAC power-down input. This pin is used to power down the IDACs or VDACs configured for power-down control.
E5	VCC1	Power	VDAC1~2 output buffers positive analog power supply. This pin must be tied to the same potential as VCC2.
E6	VDAC1	Output	VDAC1 output.
F1	A1/SDO	Input/Output	I^2C: Slave address selector. SPI: Data output.
			Data are clocked out of the input shift register on either rising or falling edges of the SCLK pin as specified by the FSDO bit.

Pin		I/O	Description
No.	Name		
F2	VIO	Power	IO supply voltage. This pin sets the I/O operating voltage for the device.
F3	VDD2	Power	Analog supply voltage. This pin must be tied to the same potential as VDD1. And it should be powered up before VCC1/2 or PVDD1/2/3/4.
F4	REFOUT	Output	Internal reference output voltage pin.
F5	VDAC2	Output	VDAC2 output.
F6	VSS1	Power	VDAC1~2 output buffers negative analog power supply. This pin must be tied to the same potential as VSS2.

Specifications

Absolute Maximum Ratings (1)

Parameter	Min	Max	Unit
VDD to GND	−0.3	6	V
Digital IO to GND	−0.3	VDD + 0.3	V
Analog IO to GND	−0.3	VDD + 0.3	
PVDD to GND	−0.3	VDD + 0.3	
VCC to VSS	−0.3	6	
Operating Temperature	−40	125	°C
Storage Temperature, Tstg		6	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	2	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
VDD[1,2]	Analog Supply Voltage	3	3.3	3.6	V
VIO	Digital IO Supply Voltage	1.65		3.6	V
PVDD[1:4]	IDAC Output Buffer Supply Voltage	1.5		VDD-0.5	V
VCC[1,2] (1)	VDAC Output Buffer Positive Supply Voltage	2.5		5.5	V
VSS[1,2] (2)	VDAC Output Buffer Negative Supply Voltage	–5.5		–2.5	V
VCC[1,2] – VSS[1,2]	VDAC Output Buffer Supply Voltage	2.5		5.5	V
TA	Operating Ambient Temperature	–40		125	°C

(1) $V_{CC\,[1,2]}$ must be connected to GND when VDACs are configured for negative output voltage range operation.
(2) $V_{SS\,[1,2]}$ must be connected to GND when VDACs are configured for positive output voltage range operation.

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
WLCSP	57	0.3	°C/W

Electrical Characteristics

All minimum/maximum specifications at T_J = –40℃ to +125℃ and all typical specifications at T_J = 25℃, $V_{DD\ [1,2]}$ = 3.0 V to 3.6 V, V_{IO} = 1.65 V to 3.6 V, $PV_{DD\ [1:4]}$ = 1.5 V to V_{DD}-0.5 V, positive output ranges: $V_{CC\ [1,2]}$ = 3.0 V to 5.5 V, $V_{SS\ [1,2]}$ = GND, negative output ranges: $V_{SS\ [1,2]}$ = –5.5 V to –3.0 V, $V_{CC\ [1,2]}$ = GND, and DAC outputs unloaded, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
VDAC Characteristics						
	Resolution		12			Bits
	Full-Scale Output Voltage Range		−2.5		0	V
			−5 0		0	V
			0		2.5	V
			0		5	V
DNL	Differential Nonlinearity	Specified 12-bit monotonic	−1	±0.5	1	LSB
INL	Integral Nonlinearity		−4	±2	4	LSB
TUE	Total Unadjusted Error	Positive output Ranges	−0.7	±0.2	0.7	%FSR
OE	Offset Error	Positive output ranges	−12	±2	12	mV
		Negative output ranges	−12	±2	12	mV
	Offset Error Temperature Drift	Positive output ranges		±5		ppm/°C
		Negative output ranges		±5		ppm/°C
GE	Gain Error	Positive output ranges	−0.5	±0.1	0.5	%FSR
		Negative output ranges	−0.5	±0.1	0.5	%FSR
	Gain Error Temperature Drift	Positive output ranges		±20		ppm/°C
		Negative output ranges		±20		ppm/°C
ZSE	Zero-Scale Error	Positive output ranges	0	2	12	mV
		Negative output ranges	−12	−2	0	mV
	Zero-Scale Error Temperature Drift	Positive output ranges		±20		ppm/°C
		Negative output ranges		±20		ppm/°C
FSE	Full-Scale Error	Positive output ranges	−0.6	±0.2	0.6	%FSR
		Negative output ranges	−0.6	±0.2	0.6	%FSR
	Full-Scale Error Temperature Drift	Positive output ranges		±20		ppm/°C
		Negative output ranges		±20		ppm/°C
CL	Capacitive Load Stability (1)	VDAC_CAP_LOAD=0	0		100	nF
		VDAC_CAP_LOAD=1	100			nF
RL	Pull-down Resistance			2		kΩ
	Output Voltage Headroom (2)	To $V_{CC[1,2]}$, IOUT = 60 mA, ΔVOUT < 5mV		0.5		V
	Output Voltage Footroom (2)	To $V_{SS[1,2]}$, IOUT = –60 mA, ΔVOUT < 5mV		0.5		V
	Short Circuit Current (2)			±75		mA

Parameter		Test Conditions	Min	Typ	Max	Unit
	DC Small Signal Output Impedance	Midscale code		0.1		Ω
Ten	Output Voltage Enable Settling Time	R_L = 2 kΩ, C_L = 200 pF, Disable to 1/2 scale settling to ±1 LSB		150		μs
Tst	Output Voltage Settling Time	R_L = 2 kΩ, C_L = 200 pF, 1/4 to 3/4 scale settling to ±1 LSB $V_{DAC\_SETTING[1:0]}$=00		30		μs
	Slew Rate	1/4 to 3/4 scale transition, 10% to 90%		0.3		V/μs
Vn	Output Noise	0.1 Hz to 10 Hz, midscale code		150		μVpp
	Output Noise Density	1 kHz, midscale code		700		nV/√Hz
PSRRac	AC PSRR	Midscale code, frequency = 1M Hz, amplitude = 100 mV PP superimposed on VDD		80		dB
		Midscale code, frequency = 1M Hz, amplitude = 100 mV PP superimposed on $V_{CC[1,2]}$		80		dB
		Midscale code, frequency = 1M Hz, amplitude = 100 mV PP superimposed on $V_{SS[1,2]}$		80		dB
PSRRdc	DC PSRR	Midscale code, ±10% variation on all supplies		0.3		mV/V
	Code Change Glitch Impulse	1 LSB change around major carrier		1		nV-s
	Code Change Glitch Amplitude	1 LSB change around major carrier		1		mV
	Channel-to-Channel DC Crosstalk	Measured DAC output at midscale, all other DAC outputs at full-scale		100		μV

All minimum/maximum specifications at T_J = –40℃ to +125℃ and all typical specifications at T_J = 25℃, $V_{DD\ [1,2]}$ = 3.0 V to 3.6 V, V_{IO} = 1.65 V to 3.6 V, $PV_{DD\ [1:4]}$ = 1.5 V to V_{DD} − 0.5 V, positive output ranges: $V_{CC\ [1,2]}$ = 3.0 V to 5.5 V, $V_{SS\ [1,2]}$ = GND, negative output ranges: $V_{SS\ [1,2]}$ = –5.5 V to –3.0 V, $V_{CC\ [1,2]}$ = GND, and DAC outputs unloaded, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
IDAC Characteristics						
	Resolution		12	12	12	Bits
	Full scale output current range		0		200	mA
DNL	Differential nonlinearity	Specified 12-bit monotonic	−1	±0.5	1	LSB
INL	Integral nonlinearity		−3	±1	3	LSB
TUE	Total unadjusted error		−1.5	±0.05	1.5	%FSR
	Offset error		−1	±0.5	1	mA
	Offset error temperature drift			±10		ppm/°C
	Gain error		−1	±0.05	1	%FSR
	Gain error temperature drift			±20		ppm/°C
	Zero-scale error		0	0.5	1	mA
	Zero-scale error temperature drift			±5		ppm/°C
	Full-scale error		−1	±0.05	1	%FSR
	Full-scale error temperature drift			±20		ppm/°C
	Output compliance voltage				PVDD – 0.3	V
	Pull down resistance (2)			2		kΩ
	Output current settling time	1/4 to 3/4 scale settling to ±1 LSB		30		µs
	Slew rate	1/4 to 3/4 scale transition, 10% to 90%		8		mA/µs
	Output noise	0.1 Hz to 10 Hz, midscale code (no ref)		2		µARMS
	Output noise density	1 kHz, midscale code (no ref)		50		nA/√Hz
	AC PSRR	Midscale code, frequency = 1M, amplitude = 20 mV PP superimposed on VDD		1000		µA/V
		Midscale code, frequency = 1M, amplitude = 20 mV PP superimposed on PVDD		1000		µA/V
	DC PSRR	Midscale code, ±10% variation on all supplies		80		dB
	Code change glitch impulse	1 LSB change around major carrier		500		pA-s
	Code change glitch amplitude	1 LSB change around major carrier		200		µA
	Channel-to-channel DC crosstalk	Measured DAC output at midscale, all other DAC outputs at full-scale		100		µA

All minimum/maximum specifications at T_J = –40℃ to +125℃ and all typical specifications at T_J = 25℃, $V_{DD\ [1,2]}$ = 3.0 V to 3.6 V, V_{IO} = 1.65 V to 3.6 V, $PV_{DD\ [1:4]}$ = 1.5 V to V_{DD}-0.5 V, positive output ranges: $V_{CC\ [1,2]}$ = 3.0 V to 5.5 V, $V_{SS\ [1,2]}$ = GND, negative output ranges: $V_{SS\ [1,2]}$ = –5.5 V to –3.0 V, $V_{CC\ [1,2]}$ = GND, and DAC outputs unloaded, unless otherwise noted.

Parameter		Test Conditions	Min	Typ	Max	Unit
ADC Characteristics						
	Resolution			12		Bits
	Full scale input voltage range		0		5	V
D_{NL}	Differential nonlinearity	Specified 12-bit monotonic	–1.5	±0.5	3.5	LSB
I_{NL}	Integral nonlinearity		–4	±1	4	LSB
	Offset error	After calibration	–6	±1	6	LSB
	Offset error match			±1		LSB
	Gain error		–0.5	±0.05	0.5	%FSR
	Gain error match			±1		LSB
	Input capacitance			12		pF
	Input bias current	ADC not converting		1		μA
	Conversion time			0.7		μs
	Acquisition time			0.3		μs
	Conversion rate				1	MSPS
Sensors Characteristics						
	VDAC current sense gain error		–0.8		0.8	%FSR
	VDAC current sense offset error	Positive output ranges	–0.5	±0.1	0.5	%FSR
		Negative output ranges	−0.5	±0.1	0.5	%FSR
	VDAC current sense accuracy			±1		%FSR
	Thermal alarm accuracy	T_J = –40°C to 150°C		±5		°C
Reference Characteristics						
V_{REFOUT}	Internal referencel voltage	T_A = 25°C	2.492	2.5	2.508	V
	Internal reference temperature coefficient	T_J = -40°C to 105°C		25		ppm/°C
	Internal reference impedance			0.5		Ω
	Internal reference output noise	0.1 Hz to 10 Hz		20		μV PP
	Internal reference noise density			200		nV/ sqrtHz
	Internal reference load current			±10		mA
	Internal reference load cap		100			nF
Digital Input Characteristics						
V_{IH}	High-level input voltage		0.7 × VIO			V
V_{IL}	Low-level input voltage				0.3 × VIO	V

Parameter		Test Conditions	Min	Typ	Max	Unit
	Input current			1		μA
	Input pin capacitance			8		pF
Digital Output Characteristics						
V_{OH}	High-level output voltage	I_{SOURCE} = 0.2 mA	VIO – 0.4			V
V_{OL}	Low-level output voltage	I_{SINK} = 0.2 mA			0.4	V
	Output pin capacitance			8		pF
V_{OL}	Open-drain low-level output voltage	I_{SINK} = 2 mA			0.4	V
Supply Monitor Characteristics						
Vcc to V_{SSTH}	Vcc to V_{SS} threshold detector	Vcc to V_{SS} supply failure detect		2		V
V_{DDTH}	V_{DD} threshold detector	V_{DD} supply failure detect		2		V
PV_{DDTH}	PVDD threshold detector	PVDD supply failure detect		1.3		V

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Parameter		Test Conditions	Min	Typ	Max	Unit
Power Consumption Characteristics						
I_{VDD}	V_{DD} supply current	No DAC load, VDACs in positive range at midscale code, IDACs at zero-scale, ADC at the fastest auto conversion rate, and static serial interface		7	9	mA
$I_{VCC[1,2]}$	V_{CC} supply current per channel			2	3.5	mA
I_{PVDD}	PVDD supply current			0.1	0.15	mA
I_{VIO}	V_{IO} supply current			1	10	μA
I_{VDD}	V_{DD} supply current	No DAC load, VDACs in negative range at midscale code, IDACs at zero-scale, ADC at the fastest auto conversion rate, and static serial interface		7	9	mA
I_{VSS}	V_{SS} supply current			2	3.5	mA
I_{PVDD}	PVDD supply current			0.1	0.15	mA
I_{VIO}	V_{IO} supply current			1	10	μA
I_{VDD}	V_{DD} supply current	ALL DACs in Power-down mode, VDACs in positive range		2.1	3	mA
I_{VCC}	V_{CC} supply current			0.06	1	mA
I_{PVDD}	PVDD supply current			0.005	0.01	mA
I_{VIO}	V_{IO} supply current			1	10	μA
I_{VDD}	V_{DD} supply current	ALL DACs in Power-down mode, VDACs in negative range		2.6	3	mA
I_{VSS}	V_{SS} supply current		−0.7	−0.5		mA
I_{PVDD}	PVDD supply current			0.005	0.01	mA
I_{VIO}	V_{IO} supply current			1	10	μA

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Parameter		Test Conditions	Min	Typ	Max	Unit
Reset Characteristics						
t_{AMCRDY}	Device ready wait time	Time for valid serial interface access, measured from reset event		100		μs
t_{RESET}	RESET pulse width			20		ns
DAC Characteristics						
	IDAC power-down response time	Measured from alarm condition, DAC outputs unloaded		100		ns
t_{DACPWD}	VDAC power-down response time			0.5		μs
	VDAC clear response time	Measured from CLEAR trigger, DAC outputs unloaded		150		ns
t_{DACCLR}	IDAC clear response time			2		μs
$t_{CLRWDTH}$	CLEAR pulse width			20		ns
$t_{LDACWDT\ H}$	LDAC pulse width			20		ns
ADC Characteristics						
$t_{ADCWAIT}$	ADC wait time	Time from when the ADC enters IDLE state to when the ADC is ready for trigger		2		μs
t_{ALMOUT}	ALARM response time	Measured from analog input out-of-range alarm condition		20		μs

Timing Requirements

All minimum/maximum specifications at T_J = –40℃ to +125℃ and all typical specifications at T_J = 25℃, $V_{DD[1,2]}$ = 3.0 V to 5.5 V, V_{IO} = 1.65 V to 5.5 V, $PV_{DD[1:4]}$ = 1.3 V to 5.5 V, positive output ranges: $V_{CC[1,2]}$ = 3.0 V to 5.5 V, $V_{SS[1,2]}$ = GND, negative output ranges: $V_{SS[1,2]}$ = –5.5 V to –3.0 V, $V_{CC[1,2]}$ = GND, and DAC outputs unloaded, unless otherwise noted.

Parameter		Min	Typ	Max	Unit
I^2C Timing Requirements					
$f_{(SCL)}$	I^2C Clock Frequency	10		400	kHz
$t_{(LOW)}$	SCL Clock Low Period	1.3			μs
$t_{(HIGH)}$	SCL Clock High Period	0.6			μs
$t_{(HDSTA)}$	Hold time after repeated start condition. After this period, the first clock is generated	0.6			μs
$t_{(SUSTA)}$	Repeated Start Condition Setup Time	0.6			μs
$t_{(SUSTO)}$	Stop Condition Setup Time	0.6			μs
$t_{(BUF)}$	Bus Free Time between Stop and Start Condition	1.3			μs
$t_{(SUDAT)}$	Data Setup Time	100			ns
$t_{(HDDAT)}$	Data Hold Time	0		900	ns
$t_{F,SDA}$	Data Fall Time	20		300	ns
$t_{F,SCL}$	Clock Fall Time			300	ns
$t_{R,SCL}$	Clock Rise Time			300	ns
$t_{R,SCL100}$	Rise Time for SCL ≤ 100 kHz			1000	ns
	SCL and SDA Timeout	20		30	ms
SPI Timing Requirements					
$f_{(SCLK)}$	SCLK Frequency			20	MHz
$t_{(SCLKHIGH)}$	SCLK High Time	23			ns
$t_{SCLKLOW}$	SCLK Low Time	23			ns
$t_{(SDISU)}$	SDI Setup Time	7			ns
$t_{(SDIHD)}$	SDI Hold Dime	7			ns
$t_{(SDOTOZ)}$	SDO Driven to Tri-State	0		15	ns
$t_{(SDOTOD)}$	SDO Tri-state to Driven	0		18	ns
$t_{(SDODLY)}$	SDO Output Delay	0		30	ns
$t_{(CSSU)}$	CS Setup Time	10			ns
$t_{(CSHD)}$	CS Hold Time	20			ns
$t_{(CSHIGH)}$	CS High Time	20			ns

(1) Values based on design and characterization.

Timing Diagrams

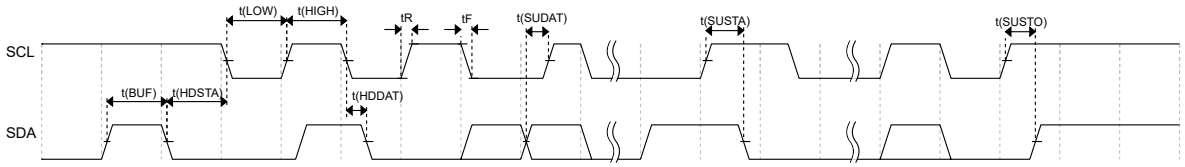


Figure 1. I²C Timing Diagram

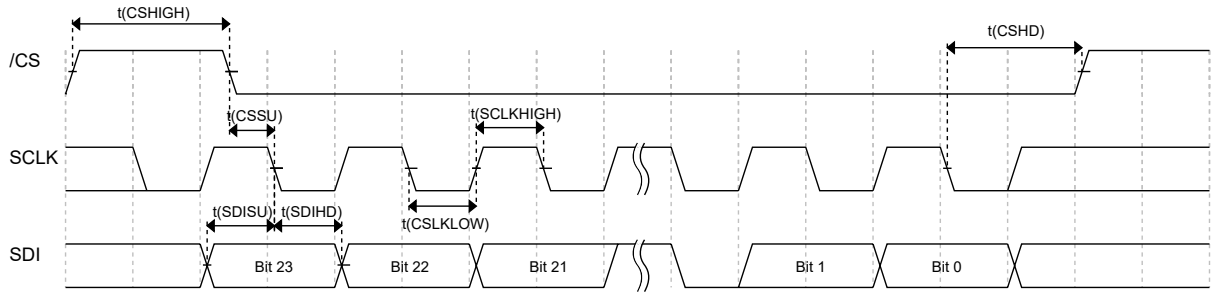


Figure 2. SPI Write Timing Diagram

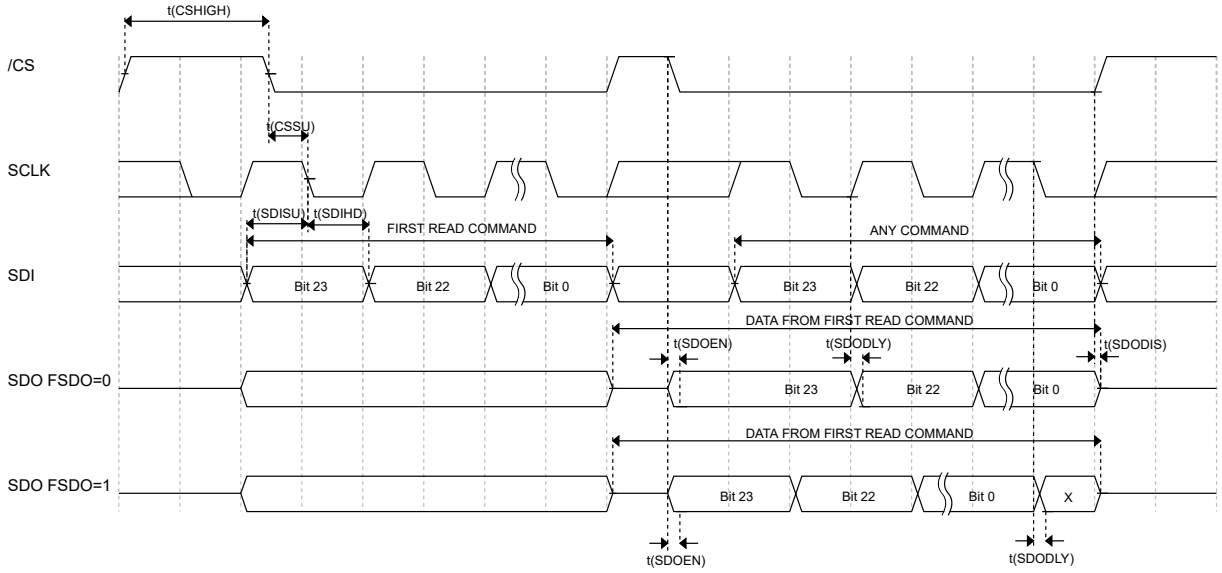


Figure 3. SPI Read Timing Diagram

Typical Performance Characteristics

All test condition: $V_{DD\ [1,2]}$ = 5 V, V_{IO} = 3.3 V, $PV_{DD\ [1:4]}$ = 3 V, positive output ranges: $V_{CC\ [1,2]}$ = 3.0 V to 5.5 V, $V_{SS\ [1,2]}$ = GND, negative output ranges: $V_{SS\ [1,2]}$ = –5 V, $V_{CC\ [1,2]}$ = GND, unless otherwise noted.

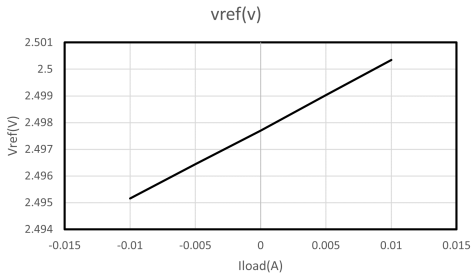


Figure 4. VREF VS Load Current

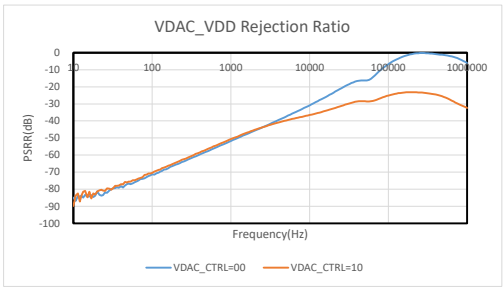


Figure 5. VDAC Rejection versus VDD

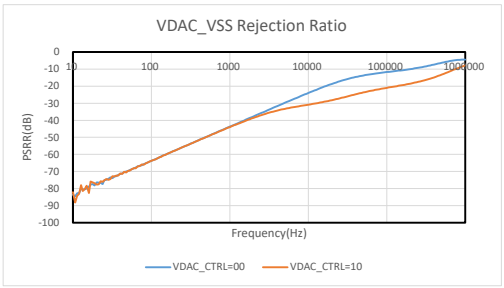


Figure 6. VDAC Rejection versus VSS

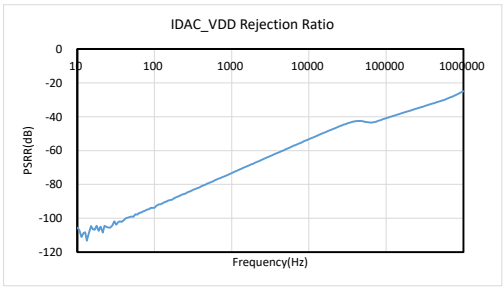


Figure 7. IDAC Rejection versus VDD

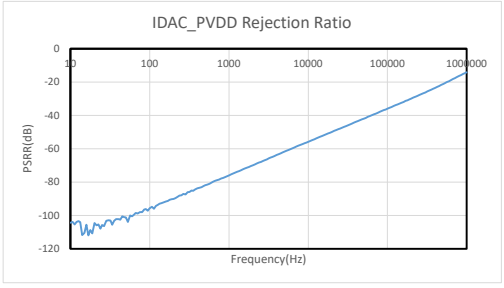


Figure 8. IDAC Rejection versus PVDD

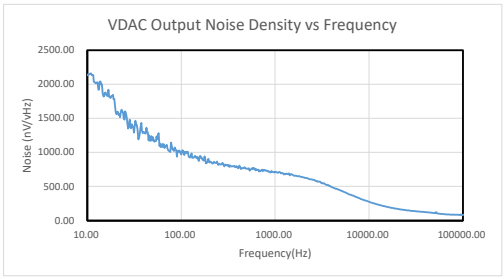


Figure 9. VDAC Noise with Cload=1

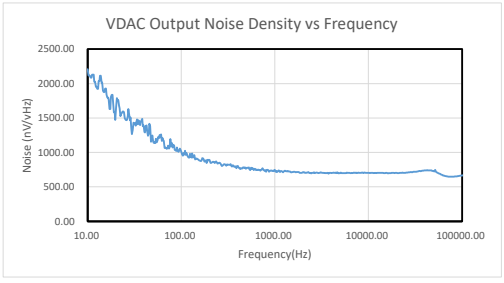


Figure 10. VDAC Noise with Cload=0

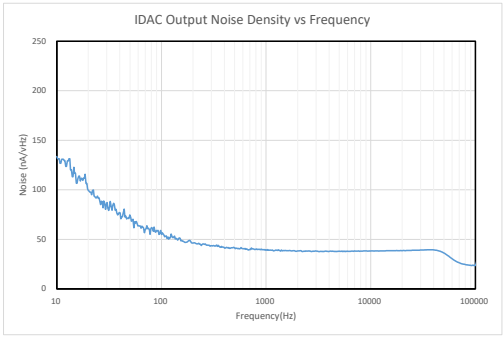


Figure 11. IDAC Noise at 200mA

Detailed Description

Overview

The TPAFEA008 is an integrated product with 4-channel negative/positive output VDAC and 4-channel IDAC, which is optimized for the optical module with 4-channel EML (Electro-absorption Modulated Laser).

Functional Block Diagram

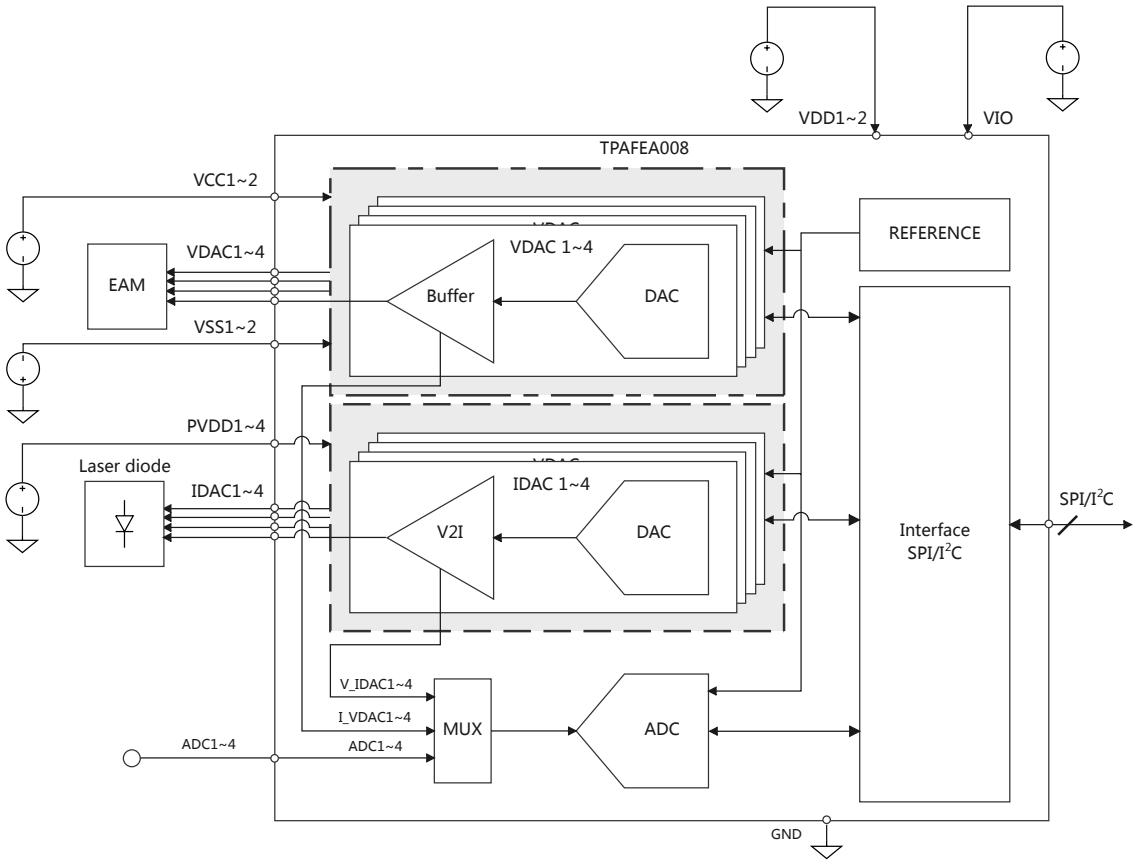


Figure 12. Functional Block Diagram

Feature Description

IDAC

The device has 4-ch IDACs.

For larger output current requirement, two or more IDAC outputs can be connected.

IDAC full range is 200 mA.

$$I_{DAC} = \frac{IDAC_{CODE}}{2^{12}} \times FSR \quad (1)$$

VDAC

The device has 4-ch VDACs which support negative or positive output range.

VDAC output current could be monitored by ADC. The full range can be configured to be 60 mA or 30 mA.

For positive output, FSR can be selected as 2.5/5 V, and VDAC equation is as followings:

$$V_{DAC} = \frac{VDAC_{CODE}}{2^{12}} \times FSR \quad (2)$$

For negative output, FSR can be selected as −2.5/−5 V, and VDAC equation is as followings:

$$V_{DAC} = \frac{VDAC_{CODE} - 2^{12}}{2^{12}} \times FSR \quad (3)$$

ADC

The ADC has 4 pins to monitor external signals and can monitor the output voltage of IDAC as well as the output current of VDAC.

For external ADC input, ADC equation is as followings, and ADC range is 2.5 V or 5 V according to register setting:

$$ADC_{CODE} = \frac{ADC_{input}}{ADC_{RANGE}} \times 2^{12} \quad (4)$$

For output voltage of IDAC, ADC equation is as followings, and ADC range is 2.5 V:

$$V_{IDAC} = \frac{ADC_{CODE}}{2^{12}} \times ADC_{RANGE} \quad (5)$$

For output current of VDAC, ADC equation is as followings:

In 30 mA range:

$$I_{VDAC} = \frac{2.5}{83.31} \times \frac{ADC_{CODE}}{2^{12}} \quad (6)$$

In 60 mA range:

$$I_{VDAC} = \frac{2.5}{41.66} \times \frac{ADC_{CODE}}{2^{12}} \quad (7)$$

Internal Reference

The device has an internal 2.5-V reference.

Alarm Function

The device has several alarm functions, including ADC alarm, overtemperature alarm, etc.

Serial Interface

The TPAFEA008 supports either I^2C-compatible two-wire bus, or an SPI-compatible bus. The device detectsbetween an SPI-compatible or I^2C -compatible master at startup, and automatically configures the interface accordingly. Protocol change during normal operation should be prevented.

The TPAFEA008 has 3 pages of registers. Address 0x01 is used to select the different pages In both SPI and I^2C configurations. The page for that register must first be selected to read and write. by writing the 5-bit representation of the page number ($PAGE_{[4:0]}$) to address 0x01. The page value is held until a new page address is programmed.

Addresses 0x00 to 0x2F on each page are global registers, thus enabling access to these bits regardless of the page configuration.

I²C Interface

In I²C mode, the device works as a slave device. The device supports the transmission protocol for fast mode. All data bytes are transmitted MSB first.

I²C Bus Overview

In I²C protocol, the device that initiates the transfer is called a master, and the devices controlled by the master are slaves.

I²C Address

The device has 4 slave addresses, which are selected by connecting the A0 and A1 pins to the VIO or GND.

Table 2. I²C Slave Address

A1	A0	Address[A6:A0]
0	0	1000000
0	1	1000001
1	0	1000010
1	1	1000011

I²C Read and Write Operation

General I²C read and write operations are supported by the device.

In the write operation, the value for the address register is the first byte transferred after the slave address byte with the R/W bit low.

In the read operation, the last value stored in the address register by a write operation is used to determine which register is read.

Reads can be repeated on the same register, and there is no need to continually send the address registerBytes.

A not-acknowledge command should be sent by master to terminate read operations at the end of the last byte to be read. At the last byte that is read from salve, the master should leave the SDA line high during the acknowledge time.

Block access functionality is provided by the device for large read and write sets. By setting the block access bit (bit 7 of register address byte) high, block access is enabled for multibyte transfers. The device reads and writes the subsequent memory locations until the transaction is terminated by the STOP condition.

I²C Timeout Function

If either SCL or SDA are held low for 25 ms (typical) between a START and STOP condition, the device resets the serial interface, releases the bus, and waits for a START condition.

To avoid activating the time-out function, make sure to maintain SCL operating frequency of at least 1 kHz.

I²C General-Call Reset

The device acknowledges the general-call address 00h (0000 0000b) and responds to the second byte. If the second byte is 06h (0000 0110b), the device executes a software reset.

SPI interface

In SPI mode, the device is controlled through a four-wire serial interface.

SPI Bus Overview

A serial interface access cycle is initiated by asserting the CS pin low and is 24 bits long. The access cycle ends when the CS pin is asserted high, so the CS pin must stay low for at least 24 SCLK falling edges.

The communication is ignored if the access cycle contains less than the minimum clock edges. The last 24 bits are used by the device If the access cycle contains more than the minimum clock edges.

When CS is high, the SCLK and SDI signals are blocked and the SDO pin is in a Hi-Z state.

SDI data are clocked in on SCLK falling edges.

Data are clocked out on the SDO pin on SCLK rising or falling edges, according to the FSDO bit setting.

Register Table

Global Register Page

There are 3 pages for TPAFEA008 register,. 1st is Global register page, 2nd is DAC register page and 3rd is ADC register page. DAC and ADC register pages are slected by PAGE_SEL bit.

In DAC resiger page, configuration registers can be set to select different range and output channels, while the followings are DAC data registers.

In ADC resiger page, configuration registers can be set to select different input channels, while the followings are ADC data registers.

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
0x00	NOP	16	[15:0]	NOP	WO	0	no operation register. Always read 0;
0x01	PAGE	16	[15:2]	RESERVED	RO	0	reserved
			[1:0]	PAGE_SEL	RW	0	0: DAC page sel; 1: ADC page sel;
0x02	CHIP_ID	16	[15:0]	CHIP_ID	RO	16'hA008	CHIP_ID
0x03	CHIP_VER	16	[15:4]	RESERVED	RO	0	reserved
			[3:0]	VERSION_ID	RO	0	VERSION ID
0x04	SW_RST	16	[15:8]	RESERVED	RO	0	reserved
			[7:0]	SW_RST	RW	0	Writing 0xA5 to this register causes a power-on-reset.
0x08	ALARM_STS0	16	[15:12]	RESERVED	RO	0	reserved
			[11:8]	ADC_ALR	RO	0	0 = corresponding ADC channel is in the normal range 1 = corresponding ADC channel is out-of-range
			[7:4]	IDAC_ALR	RO	0	
			[3:0]	VDAC_ALR	RO	0	
0x09	ALARM_STS1	16	[15:8]	RESERVED	RO	0	reserved
			[7]	OTP_ERR_ALR	RO	0	1: idac temperature is over 150°C 0: idac temperature is under 150°C

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
			[6]	OTP_WARN_ALR	RO	0	1: idac temperature is over 105°C 0: idac temperature is under 105°C
			[5]	VCC2_VSS2_ALR	RO	0	1: Voltage range from VSS to VCC is smaller than the threshold 0: Voltage range from VSS to VCC is normal
			[4]	VCC1_VSS1_ALR	RO	0	
			[3]	PVDD4_ALR	RO	0	0 = PVDD-n is no less than the PVDD threshold voltage 1 = PVDD-n is less than the PVDD threshold voltage
			[2]	PVDD3_ALR	RO	0	
			[1]	PVDD2_ALR	RO	0	
			[0]	PVDD1_ALR	RO	0	
0x0A	GLB_STS	16	[15:12]	RESERVED	RO	0	reserved
			[11:8]	VDAC_SC	RO	0	0 = The corresponding vdac has no short circuit detected 1 = The corresponding vdac has short circuit detected
			[7]	ADC_BUSY	RO	0	0 = ADC is not working; 1 = ADC is working
			[6]	RESERVED	RO	0	reserved
			[5]	VCC_VSS_GALR	RO	0	1: at least one vcc_vss has alarm event 0: no vcc_vss alarm event happened
			[4]	PVDD_GALR	RO	0	1: at least one pvdd has alarm event 0: no pvdd alarm event happened
			[3]	VDAC_GALR	RO	0	1: at least one vdac has alarm event 0: no pvdd alarm event happened
			[2]	IDAC_GALR	RO	0	1: at least one idac has alarm event 0: no idac alarm event happened
			[1]	ADC_GLAR	RO	0	1: at least one adc external channel has alarm event

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
							0: no adc external channel alarm event happened
			[0]	GALR	RO	0	1: at least one alarm has alarm event 0: no alarm event happened. Exclude VCC_VSS alarm
0x10	TRIGGER	16	[15:2]	RESERVED	RO	0	reserved
			[1]	DAC_TRIG	WO	0	Software DAC trigger. Used in DAC synchronous and self cleared.
			[0]	ADC_TRIG	R/W	0	ADC conversion trigger.
0x11	SDO_EN	16	[15:1]	RESERVED	RO	0	reserved
			[0]	SDO_EN	R/W	0	SDO Enable. SDO is enabled to read and write operations whenever the SPI CS pin is low. SDO is always disabled in I2C mode regardless of this bit set. 0 = SDO disabled; 1 = SDO enabled during read/write operations
0x12	GEN_CFG	16	[15:6]	RESERVED	RO	0	reserved
			[5]	ALARM_POL	R/W	0	0 = ALARM pin is active-low; 1 = ALARM pin is active-high
			[4]	ALARM_ODE	R/W	1	0 = ALARM pin is push-pull output; 1 = ALARM pin is open-drain output
			[3]	ALARM_LATCH_DIS	R/W	1	0 = Alarm bits are latched; 1 = Alarm bits are not latched
			[2]	CLR_PIN_EN	R/W	0	0 = LDAC/CLR pin is configured as a hardware LDAC pin; 1 = LDAC/CLR pin is configured as a hardware CLR pin

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
			[1]	FSDO	R/W	0	0 = SDO updates on SCLK rising edges, normal mode, max support 20M SCLK; 1 = SDO updates on SCLK falling edges, fast mode, max support 25M SCLK;
			[0]	SUPPLY_MONITOR	R/W	0	1: enable VDAC power supply monitor; 0: mask VDAC power supply alarm event
0x13	DAC_EN	16	[15:8]	RESERVED	RO	0	reserved
			[7:4]	IDAC_EN	W/R	0	[3:0] ~ IDAC4~1. IDAC-n power on enable
			[3:0]	VDAC_EN	W/R	0	[3:0] ~ VDAC4~1. VDAC-n power on enable
0x14	DAC_CLR	16	[15:8]	RESERVED	RO	0	reserved
			[7:4]	IDAC_CLR	W/R	0	[3:0] ~ IDAC4~1. IDAC-n clear mode enable
			[3:0]	VDAC_CLR	W/R	0	[3:0] ~ VDAC4~1. VDAC-n clear mode enable
0x15	DAC_BC	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	DAC_BC_CODE	WO	0	Writing this register will write the bc_code to all registers that enable broadcast mode
0x16	IDAC_CLR_CODE	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC_CLR_CODE	W/R	0	Clear code used in DAC clear mode;
0x17	VDAC_CLR_CODE	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC_CLR_CODE	W/R	0	Clear code used in DAC clear mode;
0x18	ALR_OUT_SRC0	16	[15:12]	RESERVED	RO	0	reserved
			[11:8]	ADC_ALR_OUT	W/R	0	[3:0] ~ ADC4~1 , 1: ADC-n alarm event will cause ALARM PAD assertion; 0: ADC-n alarm event will not cause ALARM PAD assertion.
			[7:4]	IDAC_ALR_OUT	W/R	0	[3:0] ~ IDAC4~1 ,

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
							1: IDAC-n alarm event will cause ALARM PAD assertion; 0: IDAC-n alarm event will not cause ALARM PAD assertion.
			[3:0]	VDAC_ALR_OUT	W/R	0	[3:0] ~ VDAC4~1 , 1: VDAC-n alarm event will cause ALARM PAD assertion; 0: VDAC-n alarm event will not cause ALARM PAD assertion.
0x19	ALR_OUT_SRC1	16	[15:8]	RESERVED	RO	0	reserved
			[7]	OTP_ERR_ALR_OUT	W/R	0	1: The corresponding alarm event will cause ALARM PAD assertion; 0: The corresponding alarm event will not cause ALARM PAD assertion.
			[6]	OTP_WARN_ALR_OUT	W/R	0	
			[5]	VCC2_VSS2_ALR_OUT	W/R	0	
			[4]	VCC1_VSS1_ALR_OUT	W/R	0	
			[3]	PVDD4_ALR_OUT	W/R	0	
			[2]	PVDD3_ALR_OUT	W/R	0	
			[1]	PVDD2_ALR_OUT	W/R	0	
			[0]	PVDD1_ALR_OUT	W/R	0	
0x1A	I^2C_TIMEOUT_EN	16	[15:1]	RESERVED	RO	0	reserved
			[0]	I^2C_TIMEOUT_EN	R/W	0	1: enable I^2C timeout function; 0: disable I^2C timeout function
0x20	ADC_DIS	16	[15:4]	RESERVED	RO	0	reserved
			[3:0]	ADC_DIS	RO	0	1: ADCn PAD will be used as GPIO function
0x21	GPIO_EN	16	[15:12]	RESERVED	RO	0	reserved
			[11:8]	GPIO_ODE	W/R	0	0 = GPIO pin is push-pull output; 1 = GPIO pin is open-drain output
			[7:4]	GPIO_IN_EN	W/R	0	config in_en to 0 when GPIO PAD is Hi-Z status to save Power
			[3:0]	GPIO_OUT_EN	W/R	0	config out_en to 1 to enable GPIO output mode.

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
0x22	GPIO_OUT	16	[15:4]	RESERVED	RO	0	reserved
			[3:0]	GPIO_OUT	W/R	0	The gpio_out will write to the corresponding GPIO PADs which out_en are set to 1.
0x23	GPIO_IN	16	[15:4]	RESERVED	RO	0	reserved
			[3:0]	GPIO_IN	RO	0	Read the gpio_in will read the corresponding GPIO PADs which in_en are set to 1.

DAC Register Page

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
0x30	VDAC_CTRL	16	[15:3]	RESERVED	RO	0	reserved
			[4]	VDAC_CAP_LOAD	R/W	1	1: VDAC buffer capacitive load drive capability is greater than 47nF 0: VDAC buffer capacitive load drive capability is less than 47nF
			[3:2]	VDAC34_RANGE	R/W	0	0: -5V; 1: -2.5V; 2: 5V; 3: 2.5V
			[1:0]	VDAC12_RANGE	R/W	0	0: -5V; 1: -2.5V; 2: 5V; 3: 2.5V
0x31	DAC_MODE_CFG	16	[15:12]	IDAC_BC_EN	R/W	0	enable the broadcast mode for the corresponding DAC
			[11:8]	VDAC_BC_EN	R/W	0	
			[7:4]	IDAC_SYNC_EN	R/W	0	enable the sync mode for the corresponding DAC
			[3:0]	VDAC_SYNC_EN	R/W	0	
0x32	DAC_HW_CFG	16	[15:12]	IDAC_HPD_EN	R/W	F	The corresponding DAC will enter Power-Down mode when PWDWN PAD is low;
			[11:8]	VDAC_HPD_EN	R/W	F	
			[7:4]	IDAC_HCLR_EN	R/W	F	The corresponding DAC will enter Clear mode when CLR PAD is low;
			[3:0]	VDAC_HCLR_EN	R/W	F	
0x33	DAC_APD_EN	16	[15:8]	RESERVED	RO	0	reserved
			[7:4]	IDAC_APD_EN	R/W	F	The corresponding DAC will enter Power Down mode when the Auto-Power-Down-alarm event happens.
			[3:0]	VDAC_APD_EN	R/W	F	

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
0x34	DAC_APD_SRC0	16	[15:12]	RESERVED	RO	0	reserved
			[11:8]	ADC_ALR_APD	R/W	0	1: The corresponding alr is a source of APD event 0: The corresponding alr is not a source of APD event
			[7:4]	IDAC_ALR_APD	R/W	0	
			[3:0]	VDAC_ALR_APD	R/W	0	
0x35	DAC_APD_SRC1	16	[15:8]	RESERVED	RO	0	reserved
			[7]	OTP_ERR_ALR_APD	R/W	1	1: The corresponding alr is a source of APD event 0: The corresponding alr is not a source of APD event
			[6]	OTP_WARN_ALR_APD	R/W	0	
			[5:4]	RESERVED	RO	0	reserved
			[3]	PVDD4_ALR_APD	R/W	0	1: The corresponding alr is a source of APD event 0: The corresponding alr is not a source of APD event
			[2]	PVDD3_ALR_APD	R/W	0	
			[1]	PVDD2_ALR_APD	R/W	0	
			[0]	PVDD1_ALR_APD	R/W	0	
0x40	VDAC1_BUF_REG	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC1_BUF_REG	R/W	0	vdac1 buf register, which stores the data to be loaded to the active register in sync mode
0x41	VDAC2_BUF_REG	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC2_BUF_REG	R/W	0	vdac2 buf register, which stores the data to be loaded to the active register in sync mode
0x42	VDAC3_BUF_REG	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC3_BUF_REG	R/W	0	vdac3 buf register, which stores the data to be loaded to the active register in sync mode
0x43	VDAC4_BUF_REG	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC4_BUF_REG	R/W	0	vdac4 buf register, which stores the data to be loaded to the active register in sync mode
0x44	IDAC1_BUF_REG	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC1_BUF_REG	R/W	0	Idac1 buf register, which stores the data to be loaded to the active register in sync mode
0x45	IDAC2_BUF_REG	16	[15:12]	RESERVED	RO	0	reserved

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
			[11:0]	IDAC2_BUF_REG	R/W	0	Idac2 buf register, which stores the data to be loaded to the active register in sync mode
0x46	IDAC3_BUF_REG	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC3_BUF_REG	R/W	0	Idac3 buf register, which stores the data to be loaded to the active register in sync mode
0x47	IDAC4_BUF_REG	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC4_BUF_REG	R/W	0	Idac4 buf register, which stores the data to be loaded to the active register in sync mode

ADC Register Page

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
0x30	ADC_GEN_CFG0		[15]	RESERVED	RO	0	reserved
			[14:12]	ADC_FALR_NUM	R/W	3	0: 1; 1: 4; 2: 8; 3: 16; 4: 32; 5: 64; 6: 128; 7: 256;
			[11]	RESERVED	RO	0	reserved
			[10:8]	IDAC_FALR_NUM	R/W	3	0: 1; 1: 4; 2: 8; 3: 16; 4: 32; 5: 64; 6: 128; 7: 256;
			[7]	RESERVED	RO	0	reserved
			[6:4]	VDAC_FALR_NUM	R/W	3	0: 1; 1: 4; 2: 8; 3: 16; 4: 32; 5: 64; 6: 128; 7: 256;
			[3]	RESERVED	RO	0	reserved
			[2]	CONV_MODE	R/W	1	0: one-shot-mode; 1: auto-cycle-mode
			[1]	ADC_RANGE	R/W	0	0: 5 V 1: 2.5 V
			[0]	ADC_EN	RW	1	
0x31	ADC_GEN_CFG1		[15:14]	RESERVED	RO	0	reserved
			[13:12]	AVG_NUM_ADC	R/W	0	0: 1 sample; 1: 4 samples; 2: 16 samples; 3: 64 samples
			[11:10]	AVG_NUM_IDAC	R/W	0	
			[9:8]	AVG_NUM_VDAC	R/W	0	
			[7]	DIRECTION_VDAC	R/W	0	0: source current; 1: sink current
			[6]	RNG_VDAC	R/W	0	0: 60 mA; 1: 30 mA

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
			[5:4]	CONV_ADC	R/W	0	ADC total acquisition + conversion time for one channel with no averaging. 0: 1us; 1: 4us; 2: 16us; 3: 32us;
			[3:2]	CONV_IDAC	R/W	0	ADC total acquisition + conversion time for one channel with no averaging. 0: 2us; 1: 4us; 2: 8us; 3: 16us;
			[1:0]	CONV_VDAC	R/W	0	
0x32	ADC_CSS_CFG	16	[15:14]	RESERVED	RO	0	reserved
			[13:8]	CSS_START_IDX	R/W	0	The start index pointer of channel scan sequencer
			[7:6]	RESERVED	RO	0	reserved
			[5:0]	CSS_END_IDX	R/W	B	The end index pointer of the channel scan sequencer, , which must not be lower than the start index .
0x33	BOOST_ADC	16	[15:1]	RESERVED	RO	0	reserved
			[0]	BOOST_ADC	RW	0	1: 2M SPS support 0: other SPS
0x36	ADC_HYST0	16	[15]	RESERVED	RO	0	reserved
			[14:8]	HYST_IDAC	R/W	8	Hysteresis configuration is used for threshold comparison of alarm logic of IDAC
			[7]	RESERVED	RO	0	reserved
			[6:0]	HYST_VDAC	R/W	8	Hysteresis configuration is used for threshold comparison of alarm logic of VDAC
0x37	ADC_HYST1	16	[15]	RESERVED	RO	0	reserved
			[14:8]	HYST_ADC2	R/W	8	Hysteresis configuration is used for threshold comparison of alarm logic of ADC2
			[7]	RESERVED	RO	0	reserved
			[6:0]	HYST_ADC1	R/W	8	Hysteresis configuration is used for threshold

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
							comparison of alarm logic of ADC1
0x38	ADC_HYST2	16	[15]	RESERVED	RO	0	reserved
			[14:8]	HYST_ADC4	R/W	8	Hysteresis configuration is used for threshold comparison of alarm logic of ADC4
			[7]	RESERVED	RO	0	reserved
			[6:0]	HYST_ADC3	R/W	8	Hysteresis configuration is used for threshold comparison of alarm logic of ADC3
0x40	VDAC1_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC1_UP_TH	RW	12'hFFF	upper threshold for the VDAC1 channel of ADC
0x41	VDAC1_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC1_LO_TH	RW	0	lower threshold for VDAC1 channel of ADC
0x42	VDAC2_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC2_UP_TH	RW	12'hFFF	upper threshold for the VDAC2 channel of ADC
0x43	VDAC2_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC2_LO_TH	RW	0	lower threshold for VDAC2 channel of ADC
0x44	VDAC3_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC3_UP_TH	RW	12'hFFF	upper threshold for the VDAC3 channel of ADC
0x45	VDAC3_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC3_LO_TH	RW	0	lower threshold for VDAC3 channel of ADC
0x46	VDAC4_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC4_UP_TH	RW	12'hFFF	upper threshold for the VDAC4 channel of ADC
0x47	VDAC4_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	VDAC4_LO_TH	RW	0	lower threshold for VDAC4 channel of ADC
0x48	IDAC1_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC1_UP_TH	RW	12'hFFF	upper threshold for IDAC1 channel of ADC
0x49	IDAC1_LO_TH	16	[15:12]	RESERVED	RO	0	reserved

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
			[11:0]	IDAC1_LO_TH	RW	0	lower threshold for IDAC1 channel of ADC
0x4A	IDAC2_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC2_UP_TH	RW	12'hFFF	upper threshold for IDAC2 channel of ADC
0x4B	IDAC2_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC2_LO_TH	RW	0	lower threshold for IDAC2 channel of ADC
0x4C	IDAC3_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC3_UP_TH	RW	12'hFFF	upper threshold for IDAC3 channel of ADC
0x4D	IDAC3_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC3_LO_TH	RW	0	lower threshold for IDAC3 channel of ADC
0x4E	IDAC4_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC4_UP_TH	RW	12'hFFF	upper threshold for IDAC4 channel of ADC
0x4F	IDAC4_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	IDAC4_LO_TH	RW	0	lower threshold for IDAC4 channel of ADC
0x50	ADC1_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC1_UP_TH	RW	12'hFFF	upper threshold for ADC1 channel of ADC
0x51	ADC1_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC1_LO_TH	RW	0	lower threshold for ADC1 channel of ADC
0x52	ADC2_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC2_UP_TH	RW	12'hFFF	upper threshold for ADC2 channel of ADC
0x53	ADC2_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC2_LO_TH	RW	0	lower threshold for ADC2 channel of ADC
0x54	ADC3_UP_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC3_UP_TH	RW	12'hFFF	upper threshold for ADC3 channel of ADC
0x55	ADC3_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC3_LO_TH	RW	0	lower threshold for ADC3 channel of ADC
0x56	ADC4_UP_TH	16	[15:12]	RESERVED	RO	0	reserved

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
			[11:0]	ADC4_UP_TH	RW	12'hFFF	upper threshold for ADC4 channel of ADC
0x57	ADC4_LO_TH	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC4_LO_TH	RW	0	lower threshold for ADC4 channel of ADC
0x60	ADC_CSS_TBL0	16	[15:12]	CSS_ID3	R/W	3	ADC Channel Select Sequencer index setting: 0: VDAC1; 1: VDAC2; 2: VDAC3; 3: VDAC4; 4: IDAC1; 5: IDAC2; 6: IDAC3; 7: IDAC4; 8: ADC1; 9: ADC2; 10: ADC3; 11: ADC4;
			[11:8]	CSS_ID2	R/W	2	
			[7:4]	CSS_ID1	R/W	1	
			[3:0]	CSS_ID0	R/W	0	
0x61	ADC_CSS_TBL1	16	[15:12]	CSS_ID7	R/W	7	
			[11:8]	CSS_ID6	R/W	6	
			[7:4]	CSS_ID5	R/W	5	
			[3:0]	CSS_ID4	R/W	4	
0x62	ADC_CSS_TBL2	16	[15:12]	CSS_ID11	R/W	11	
			[11:8]	CSS_ID10	R/W	10	
			[7:4]	CSS_ID9	R/W	9	
			[3:0]	CSS_ID8	R/W	8	
0x63	ADC_CSS_TBL3	16	[15:12]	CSS_ID15	R/W	0	
			[11:8]	CSS_ID14	R/W	0	
			[7:4]	CSS_ID13	R/W	0	
			[3:0]	CSS_ID12	R/W	0	
0x64	ADC_CSS_TBL4	16	[15:12]	CSS_ID19	R/W	0	
			[11:8]	CSS_ID18	R/W	0	
			[7:4]	CSS_ID17	R/W	0	
			[3:0]	CSS_ID16	R/W	0	
0x65	ADC_CSS_TBL5	16	[15:12]	CSS_ID23	R/W	0	
			[11:8]	CSS_ID22	R/W	0	
			[7:4]	CSS_ID21	R/W	0	
			[3:0]	CSS_ID20	R/W	0	
0x66	ADC_CSS_TBL6	16	[15:12]	CSS_ID27	R/W	0	
			[11:8]	CSS_ID26	R/W	0	
			[7:4]	CSS_ID25	R/W	0	
			[3:0]	CSS_ID24	R/W	0	
0x67	ADC_CSS_TBL7	16	[15:12]	CSS_ID31	R/W	0	
			[11:8]	CSS_ID30	R/W	0	
			[7:4]	CSS_ID29	R/W	0	
			[3:0]	CSS_ID28	R/W	0	

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
0x68	ADC_CSS_TBL8	16	[15:12]	CSS_ID35	R/W	0	
			[11:8]	CSS_ID34	R/W	0	
			[7:4]	CSS_ID33	R/W	0	
			[3:0]	CSS_ID32	R/W	0	
0x69	ADC_CSS_TBL9	16	[15:12]	CSS_ID39	R/W	0	
			[11:8]	CSS_ID38	R/W	0	
			[7:4]	CSS_ID37	R/W	0	
			[3:0]	CSS_ID36	R/W	0	
0x6A	ADC_CSS_TBL10	16	[15:12]	CSS_ID43	R/W	0	
			[11:8]	CSS_ID42	R/W	0	
			[7:4]	CSS_ID41	R/W	0	
			[3:0]	CSS_ID40	R/W	0	
0x6B	ADC_CSS_TBL11	16	[15:12]	CSS_ID47	R/W	0	
			[11:8]	CSS_ID46	R/W	0	
			[7:4]	CSS_ID45	R/W	0	
			[3:0]	CSS_ID44	R/W	0	
0x70	ADC_VDAC1_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_VDAC1_DATA	RO	0	ADC conversion result of vdac1 channel
0x71	ADC_VDAC2_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_VDAC2_DATA	RO	0	ADC conversion result of vdac2 channel
0x72	ADC_VDAC3_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_VDAC3_DATA	RO	0	ADC conversion result of vdac3 channel
0x73	ADC_VDAC4_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_VDAC4_DATA	RO	0	ADC conversion result of vdac4 channel
0x74	ADC_IDAC1_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_IDAC1_DATA	RO	0	ADC conversion result of idac1 channel
0x75	ADC_IDAC2_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_IDAC2_DATA	RO	0	ADC conversion result of idac2 channel
0x76	ADC_IDAC3_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_IDAC3_DATA	RO	0	ADC conversion result of idac3 channel
0x77	ADC_IDAC4_DATA	16	[15:12]	RESERVED	RO	0	reserved

Address	RegName	Width	Bit	FieldName	R/W	ResetValue	Description
			[11:0]	ADC_IDAC4_DATA	RO	0	ADC conversion result of idac4 channel
0x78	ADC_ADC1_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_ADC1_DATA	RO	0	ADC conversion result of adc1 channel
0x79	ADC_ADC2_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_ADC2_DATA	RO	0	ADC conversion result of adc2 channel
0x7A	ADC_ADC3_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_ADC3_DATA	RO	0	ADC conversion result of adc3 channel
0x7B	ADC_ADC4_DATA	16	[15:12]	RESERVED	RO	0	reserved
			[11:0]	ADC_ADC4_DATA	RO	0	ADC conversion result of adc4 channel

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPAFEA008 is supplied by several voltages, in which VDD1/2 (analog supply) should be powered up before VCC1/2 (VDAC supply) or PVDD1/2/3/4 (IDAC supply).

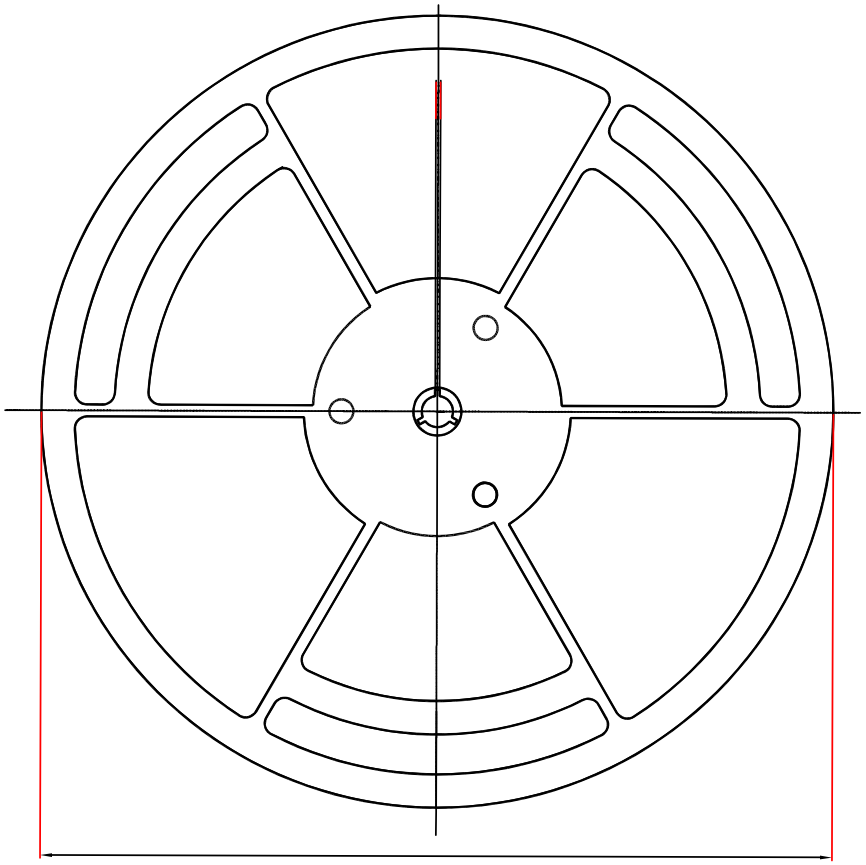
The TPAFEA008 has a protection strategy to prevent un-expected writing to config register in normal operation, so if customer want to change DAC range, make sure DAC is disabled and then change DAC range register. Writing operation to DAC range register will be ignored when DAC is enabled.

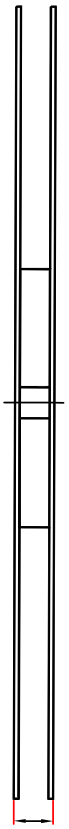
Layout

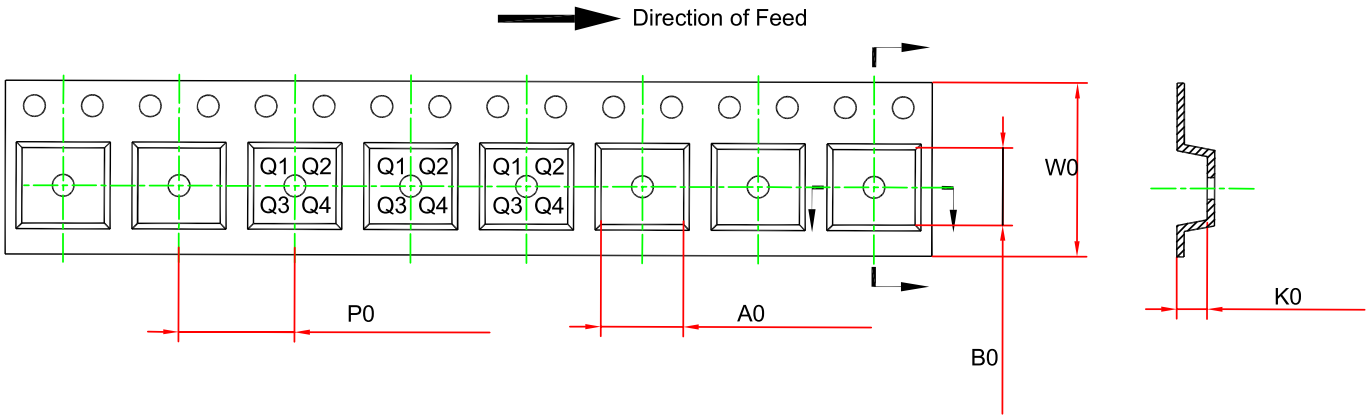
Layout Guideline

- Both input capacitors and output capacitors must be placed to the device pins as close as possible.
- It is recommended to bypass the input pin to ground with a 0.1-μF bypass capacitor.
- It is recommended to use wide and thick copper to minimize I×R drop and heat dissipation.
- Exposed pad must be connected to the PCB ground plane directly, the copper area must be as large as possible.

Tape and Reel Information





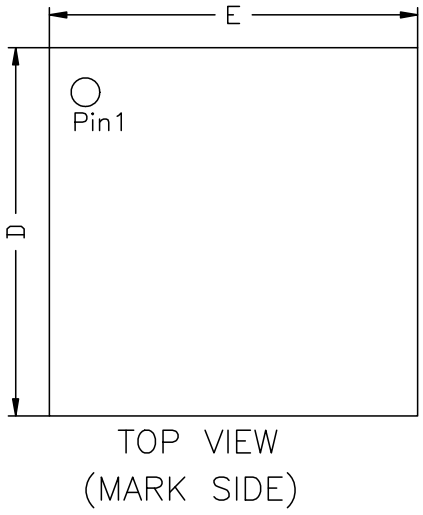


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPAFEA008-WLPR	WLCSP	175.0	12.4	2.7	2.7	0.57	4.0	12.0	Q1

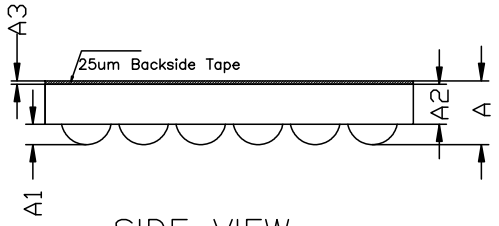
Package Outline Dimensions

WLCSP

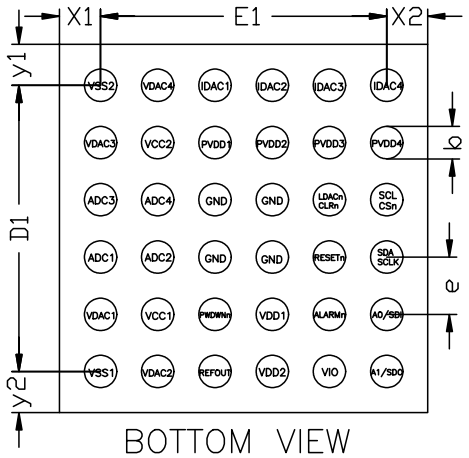
Package Outline Dimensions WLP(WLCSP-A)



TOP VIEW
(MARK SIDE)



SIDE VIEW



BOTTOM VIEW
(BALL SIDE)

NOTES
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SYMBOL	MIN	NOM	MAX
A	0.399	0.447	0.495
A1	0.122	0.142	0.162
A2	0.255	0.280	0.305
A3	0.022	0.025	0.028
D	2.545	2.575	2.605
D1		2.000BSC	
E	2.545	2.575.	2.605
E1		2.000BSC	
b	0.207	0.227	0.247
e		0.400BSC	
x1		0.2875 REF	
x2		0.2875 REF	
y1		0.2875 REF	
y2		0.2875 REF	

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPAFEA008-WLPR	−40 to 125°C	WLCSP	008	1	Tape and Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

IMPORTANT NOTICE AND DISCLAIMER

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

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