EPCS4001

Radiation and magnetic tolerant buck converter control IC

Features
- Optimized for GaN-based power stage EPC7011.
- CERN-designed rad-hard CMOS controller ASIC.
- Input voltage range 17V to 48 V.
- Integrated 5V and 12V regulators for bias supply of the power stage.
- Adjustable switching frequency 0.5-3MHz.
- High bandwidth feedback loop (100KHz) for fast transient performance.
- Under-voltage lockout.
- Over-Temperature protection.
- Power Good output.
- Enable Input.

Applications
Point Of Load in distributed power systems where radiation tolerance is required.

Description
EPCS4001 is a 48V-input buck converter controller with 12V nominal (adjustable) output voltage. This converter is developed to provide an efficient solution for DC power conversion and distribution in space applications and High Energy Physics systems. As such, it has been designed for flawless functionality in harsh radiation and magnetic field environments.

EPCS4001 has been developed to work seamlessly with the EPC7011 and EPC 7009 family of GaN ePower stage and drivers from EPC Space.

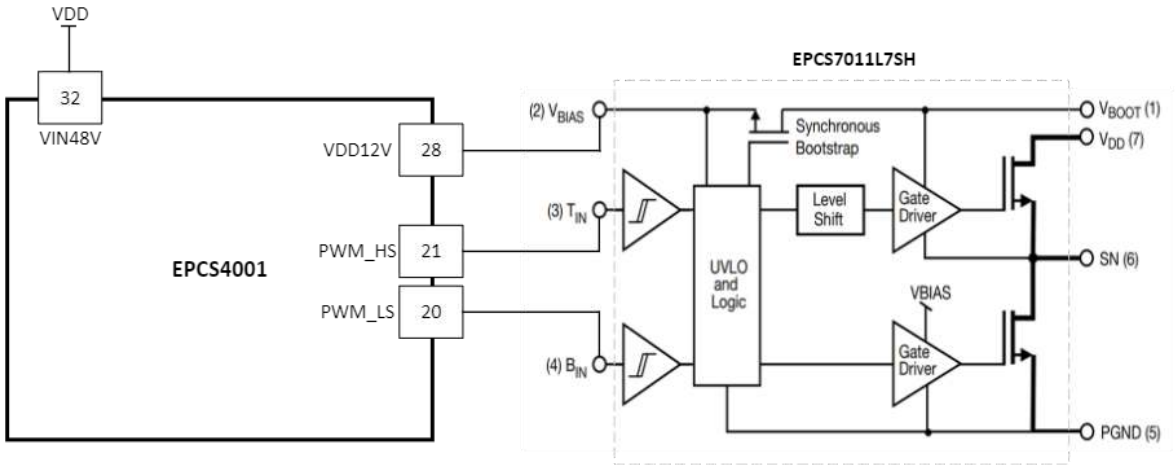
The selection of appropriate CMOS technology, coupled to the systematic use of Radiation Hardness by Design (RHBD) techniques, makes the controller capable of continuous operation up to very high radiation limit (50Mrad and 4e14 n/cm2 and 2.23e14 p/cm2(30MeV proton beam). The controller has been designed for operation in a strong magnetic field in excess of 40,000 Gauss and has been optimized for cored and coreless inductors of 200-500nH. To be compatible with these small inductance values, its switching operation is in the 0.5-3MHz range.

The controller integrates two linear regulators that generate the supply voltages for the power stage without external active components: LinPOL48V and LinPOL12V. LinPOL48V output can be adjusted and has a nominal value of 12V, while LinPOL12V provides a fixed 5V output from 12V. Both regulators can be enabled separately.

Protection features include Over-Temperature and Input Under-Voltage to improve system-level security in the event of fault conditions. The chip temperature increase in the application can be monitored via a dedicated analog signal (PTAT). Power good open drain output is available.

Main application for the EPCS4001 is the DC-DC conversion from 48V to 12V, as shown in the typical application diagram.

Simplified application block diagram



Absolute Maximum Ratings

Absolute maximum rating limits beyond which damage to the device may occur and reliability may be compromised. All voltages referred to GND.

Input Voltage Vin48V……..……..…-0.3V to +50.0V
DiodeK……..……..…-0.3V to +70.0V
DiodeA……..……..…-0.3V to +70.0V
SW Voltage……..-2.5 V to Vin48V+2.5V
SW_Clamp Voltage……..……..-2.5 V to Vin48V+2.5V
Vout Voltage……..……..…0.3 V to 24V
OutLin Voltage……..…-0.3V to +14V
VDD12V Voltage…..……..……..-0.3V to +13V
VDD5V Voltage……..……..……..-0.3V to +5.5V
Vin control Vin_ctrl……..……..-0.3V to +13V
Feedback input Voltage of the E/A Vi……..…-0.3V to +3.6V
Frequency selector Rf……..…-0.3V to +3.6V
VoutS voltage ……..…-0.3V to +3.6V
Buck_En ……..……..……..-0.3V to +3.6V
Power good ……..……..…-0.3V to +3.6V
Current in PGood pin (when PGood is negated)……..…500uA
Feedback input Voltage of the E/A Vi……..…-0.3V to +3.6V
Frequency selector Rf……..…-0.3V to +3.6V
VoutS voltage ……..…-0.3V to +3.6V
Controller Enable ……..……..……..-0.3V to +3.6V
Power good ……..……..…-0.3V to +3.6V
VDD5V_En ……..……..…-0.3V to +3.6V
VDD12V_En ……..……..…-0.3V to +3.6V

Pins Configuration and internal diodes

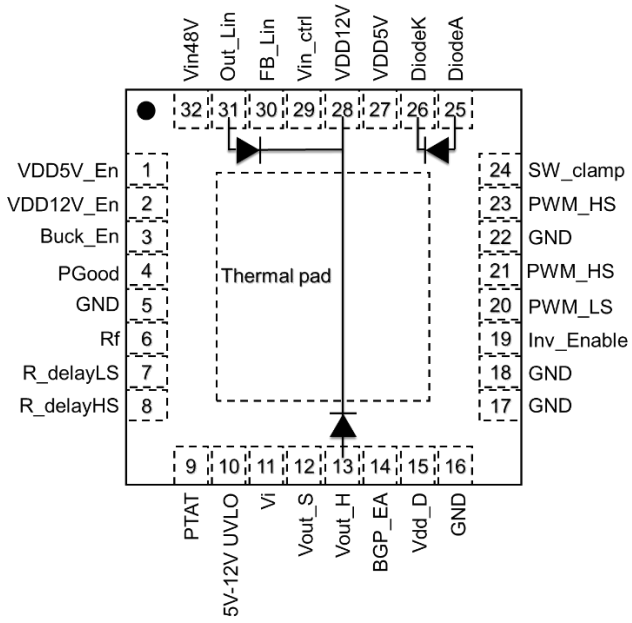


Figure 1. Pins configuration

Pins Functional description

VDD5V_En (Pin 1): LinPOL12V (5V output) enable input. The linear regulator from the Vin_ctrl to 5V output is normally on, as this pin is connected to an internal pull-up at 3.3V. Connect this pin to ground to disable the regulator. A 1uF ceramic capacitor shall be placed between VDD5V (Pin 27) and ground for linear regulator stability, if LinPOL12V (5V output) is enabled,

VDD12V_En (Pin 2): LinPOL48V (12V output) enable input. In order to ensure a proper startup in all conditions, a 24kΩ resistor from pin 2 to ground should be used. This resistor, in combination with the internal 500kΩ pullup resistor, enables LinPOL48V when Vin48V is above 17V, thus ensuring that Vin48V is above the minimum value. Connect this pin to ground to disable the regulator. A 1uF ceramic capacitor shall be placed between VDD12V (Pin 28) and ground for linear regulator stability, if LinPOL48V (12V output) is enabled,

Buck_En (Pin 3): Buck Enable input. EPCS4001 is normally disabled and requires a voltage above 0.8V applied to this pin to be enabled and start operation. This voltage has been chosen to make the pin compatible with control from any input between 0.9 and 3.3V. In order to turn off, EPCS4001 Enable pin must be lowered below 500mV. The polarity of the pin can be inverted by connecting Inv_Enable (Pin19) to GND, in which case EPCS4001 is enabled when pin voltage is below 0.5V and disabled when pin voltage exceeds 0.8V. Note that an embedded 500 kΩ resistor pulls the voltage of the Buck_En pin to GND.

PGood (Pin4): Power Good flag. This open-drain output pin conducts when EPCS4001 is not regulating the output voltage. It requires a pull-up resistor to the appropriate user-required voltage. It is recommended to obtain this voltage from Vout, either with a simple pull-up or with a voltage divider, to control the power good voltage range for example below 3.3V. The value of the pull-up resistor determines the current in the open-drain NMOS, which shall never exceed 0.5mA. PGood is asserted (NMOS off) during normal operation, while it is negated (NMOS on) in disabled mode, during restart, in case of under-voltage or over-temperature, and when the output voltage is outside a regulation window of approximately ±6.5% with respect to the selected Vout.

GND (Pin 5,16,17,18,22): Ground of the control electronics of the controller. It must be connected to the PCB ground power plane as close as possible to the power stage GND in a single point (star connection), in such a way to prevent high amplitude pulsed current to interfere with the control circuit. Please refer to the recommended layout for further details.

Rf (Pin 6): Frequency Selector. A resistor placed between this Pin and the GND determines the switching frequency of the controller, as illustrated in the following table.

Resistance (Ohm)	Frequency (MHz)
270K	1.03
200K	1.35
180K	1.48
160K	1.65
130K	1.99
100K	2.51
82K	2.98

R_delayLS (Pin 7) and R_delayHS (Pin 8): Resistors to set the dead time by defining the delays of the low side (td_OFF) and high side (td_ON) turn on times, The table below shows td_ON and td_OFF as a function of the resistors value.

Rdelay [kOhm]	td_ON / td_OFF[ns]
18	3.5
27	4.5
47	6.5
75	9.5
82	10
91	11
120	14
150	16.5

PTAT (Pin 9): Proportional-To-Absolute Temperature, it provides a voltage proportional to the variation of the chip internal temperature. The voltage at room temperature is around 500mV, with a large variability from chip to chip; the slope typical value is 8.5 mV/ºC.

5V-12V UVLO (Pin 10): UVLO level selection pin, internally pulled up to 3.3V. When this pin is unconnected, the UVLO levels for Vin_Ctrl are 10.5V rising and 9.5V falling. When this pin is connected to ground Vin_Ctrl UVLO levels are 4.5V rising and 4V falling. This pin, in combination with the 5V regulator, provides compatibility with power stages using 5V logic power supplies.If this pin is connected to ground, LinPOL12V must be enabled (please refer to VDD5V_En, Pin 1)

Vi (Pin 11): Input voltage of the Error Amplifier. The compensation network is integrated on-chip and ensures a bandwidth of about 100kHz, but the DC regulation voltage Vout is selected by the addition of 2 voltage dividers between Vout and ground, as shown in Figure 2. The two voltage dividers are necessary because the ESD protections connected to the feedback nodes are rated at 3.3V maximum. A first voltage divider (composed by Rout1 and Rout2) will scale down the Vout voltage to a "scaled" voltage Vout_S in a range between 1.5V and 3.3V. Vi is connected at the second voltage divider and the resulting voltage is compared to the internal reference voltage (about 0.58V). The resistor between Vout_S and Vi must have a value of 1MΩ, while the one between Vi and ground is selectable (including not populating it, therefore Vout_S=Vref=0.58V). Rout1 and Rout2 must be lower than 50Kohm in value to avoid issues in the compensation network. To set Vout=12V the following resistor values are recommended: Rout1=11KOhm, Rout2=3.3KOhm, Ri=262KOhm.
If Vout is below 3.3V the voltage divider Rout1/Rout2 is not required.

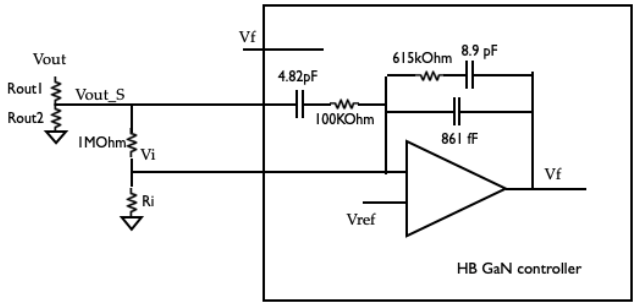


Figure 2: Configuring the output voltage.

Vout_S (Pin 12): 3.3V-level scaled-down of converter output voltage Vout, to be compatible with the ESD protections. See **Vi (Pin 11)** description**.**

Vout_H (Pin 13): Vout voltage recirculation input, connected to VDD12V through a diode. This connection allows to improve the efficiency by supplying the power stage from the output voltage, instead of using the linear regulator, when Vout is higher than OutLin. This methodology can be used only when Vout is set below 13V (to avoid exceeding the power stage maximum supply voltage) and Out_Lin set lower than Vout by adjusting the resistor divider in FB_Lin (pin 32).

During startup, when the output of the converter is low, the internal linear regulator will provide the 12V required trough the diode between Out_Lin and VDD12V. As soon as the output voltage exceeds Out_Lin, VDD is supplied from Vout_H, which prevents unnecessary power dissipation in the on-chip linear regulator. In order to ensure that Vout takes over, Out_Lin should be set to approximately 11.5V for Vout=12V, please refer to FB_Lin (30) description.
If Vout recirculation is not used, this pin can be left floating.

Bgp_EA (Pin 14): The reference voltage to the Error Amplifier is buffered and made observable at this pin exclusively for test purposes. This pin should never be used and left unconnected in final applications.

Vdd_D (Pin 15): internal 3.3V voltage regulator outputs, made observable at this pin exclusively for test purposes. This pin should never be used and left unconnected in final applications.

Inv_Enable (Pin 19): Connect to GND to change the polarity of the **Buck_En (Pin 3)** pin. If not used, it is recommended to leave this pin unconnected.

PWM_LS (Pin 20): Low side (LS) PWM gate signal (0 to 3.3V swing) to be connected to suitable input of gate driver or power stage.

PWM_HS (Pins 21, 23): High side (HS) PWM gate signal (0 to 3.3V swing) to be connected to suitable input of gate driver or power stage.

SW_clamp (Pin24): To be connected to SW node. The clamping circuit draws current from this pin when the controller is disabled, to ensure that the output voltage does not rise uncontrolled when both HS and LS switches are off and there is no load connected to the converter. This pin has a resistive behavior with a slope of 4kΩ, and saturates at around 5mA when the voltage in the SW_clamp pin is greater than 20V, as shown in Figure 3. When the controller is enabled, the leakage current is smaller than 0.5µA. If not required by the application, this pin can be left unconnected.

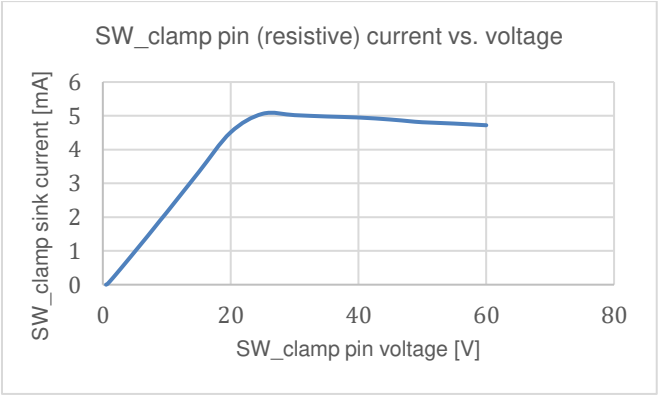


Figure 3: Pin24 resistive characteristic. Controller disabled.

DiodeA (Pin25): Anode of the floating, high speed diode. To be used as a bootstrap diode if a power stage without integrated diode is used, and connected to viable gate drive supply.

DiodeK (Pin26): Cathode of the floating, high speed diode. To be connected to the bootstrap capacitor. Please note that this pin experiences the bootstrap voltage with the high dynamics switching node (SW) voltage superimposed, including the HS switch reverse conduction during td_ON, in case of negative inductor current. Therefore, to prevent overvoltage and ensure a reliable operation, an RC filter must be added to this pin, as shown on Fig. 4.

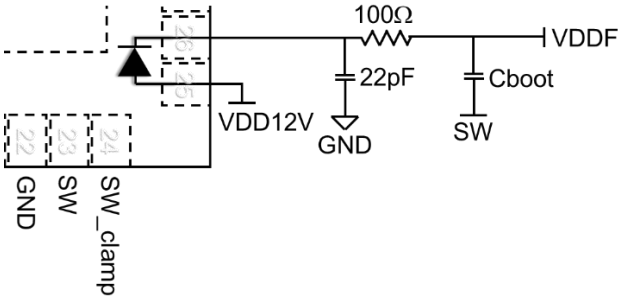


Figure 4: Filter for high frequency spikes on DiodeK.

VDD5V (Pin 27): Fixed 5V output from 12V bias supply linear regulator. This regulator is provided for compatibility with GaN power stages using a 5V logic power supply. Please refer to **5V-12V UVLO (Pin 10)** description. A 1uF ceramic capacitor shall be placed between this pin and ground for linear regulator stability, if LinPOL12V (5V output) is enabled (please refer to VDD5V_En Pin 1)

VDD12V (Pin 28): Please refer to **Out_Lin (Pin30)** specifications. This is the 12V bias supply line to gate driver or power stage. A 1uF ceramic capacitor shall be placed between this pin and ground for linear regulator stability, if LinPOL48V (12V output) is enabled (please refer to VDD12V_En Pin 2)

Vin_ctrl (Pin29): Supply voltage for the internal control circuitry. This pin is usually connected to the same voltage as the GaN power stage logic power supply (VDD12V pin). The 3.3V internal linear regulator starts up when Vin_ctrl is higher than 4.2V. The soft start procedure starts when the voltage on this pin is higher than the UVLO level configured by **5V-12V UVLO (Pin 10)**, and the **Buck_En (Pin 3)** is active.

FB_Lin (Pin 30): This is the feedback signal of the LinPOL48V block. It is internally connected to a voltage divider to regulate 12V at the Out_Lin pin as default. The setpoint can be changed using an external voltage divider connected to VDD12V, as shown on Figure 5. The output voltage can be calculated as:

$$VDD12V = Vref\frac{R1 + R2}{R2}$$

with Vref = 1.22V typical.

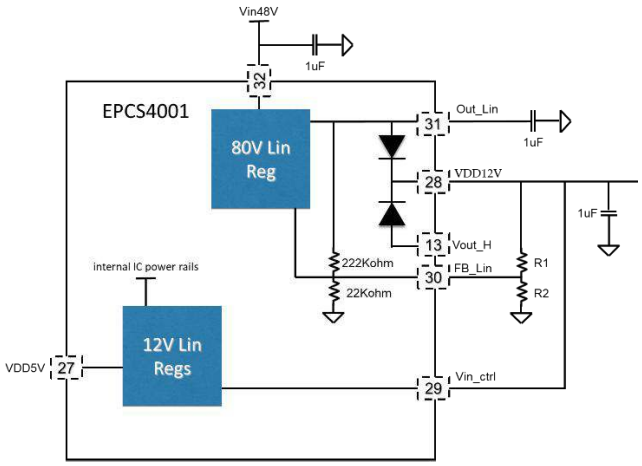


Figure 5: Internal regulators structure.

Out_Lin (Pin31): Output of the linear regulator from Vin48V. The maximum current available from this on-chip regulator is 100mA. A 1uF ceramic capacitor shall be placed between Out_Lin and GND.

Vin48V (Pin32): This input is connected to the LinPOL48V linear regulator, to internally generate the rest of the voltages for the controller and the supply of the powerstage. It should be connected to the input voltage of the converter, with a decoupling 1uF ceramic capacitor placed as close as possible to the chip.

Recommended Operating Conditions

Description	Min	Max	Unit
Input voltage - Vin	13	48	V
Output voltage - Vout	0.6	24	V
Conversion ratio - Vout/Vin (min on time 40ns)	2	20	
Switching frequency	0.5	3	MHz
Enable voltage		3.3	V
Power Good voltage		3.3	V

Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power						
Vin	Input voltage supply range	Controller operational	13		48	V
Iin	Input bias current for internal IC circuitry	En pin low, controller disabled	-	4.5	-	mA
		Enabled, 3MHz switching frequency	-	6	-	mA
PWM						
DMax	Maximum Duty Cycle		-	97	-	%
DMin	Minimum Duty Cycle		-	0	-	%
ton min	Minimum on pulse width	Smallest PWM width (except 0ns)		40		ns
Error Amplifier						
DCG	DC Gain	CL = 1pF at VF Pin	-	90	-	dB
UGBW	Unity Gain-Bandwidth	CL = 1pF at VF Pin	-	20	-	MHz
SR	Slew Rate	CL = 1pF at VF Pin	-	10	-	V/µs
Under-Voltage Lockout						
VinStartTh	Vin to enable OutLin	Vin rising trip level, R=24kΩ between pin 2 and GND	-	17	-	V
Vin_ctrl_Start_th	Vin_Ctrl to enable the internal 3.3V regulators. Rising	Vin_Ctrl rising trip level	-	3.4	-	V
Vin_ctrl_Stop_th	Vin_Ctrl to disable the internal 3.3V regulators. Falling	Vin_Ctrl falling trip level	-	3.1	-	V
Enable						
EnStartTh	Enable start threshold	Enable rising trip level	-	800	-	mV
EnStopTh	Enable stop threshold	Enable falling trip level	-	720	-	mV
EnSerRes	Enable pin series resistance (to limit current through ESD when EPCS4001 is not powered)		-	10	-	kΩ
EnPullDownRes	Embedded Enable resistor to GND		-	500	-	kΩ

Protections						
OTPStartTh	Over Temperature Protection start threshold	Tj rising trip level	-	120	-	ºC
OTPStopTh	Over Temperature Protection stop threshold	Tj falling trip level	-	80	-	ºC
SW_Clamp						
Iclamp	Clamping current	Controller disabled. Voltage at the SW_Clamp pin = 2V		0.3		mA
Ileak	Leakage in the SW_Clamp pin	Controller enabled. Voltage in the SW_Clamp pin = 60V		0.5		uA
Soft Start						
SSt	Duration of Soft Start to reach regulation at nominal Vout	f=2MHz		400		us
		f=3MHz		250		us
SSt_ton_min	Min ON time of PWM_HS during soft start		21			ns
Power Good						
OV	Output Over Voltage PGood upper threshold	With respect to nominal output		+6.5		%
UV	Output Under Voltage PGood lower threshold	With respect to nominal output		-6.5		%
Proportional To Absolute Temperature signal						
PTAT	Analog output voltage	Controller disabled, by characterization		8.5		mV/ºC
Rth	Thermal Rresistance	Temperature of the chip measured with PTAT and bottom plate temperature measured with thermocouple.		10		ºC/W

Radiation characteristics

The waveforms and characteristics corresponding to the total ionizing dose (TID), single event effects (SEE) and displacement damage (DD) tests are shown in the **typical waveforms and characteristics** section.

Block Diagram

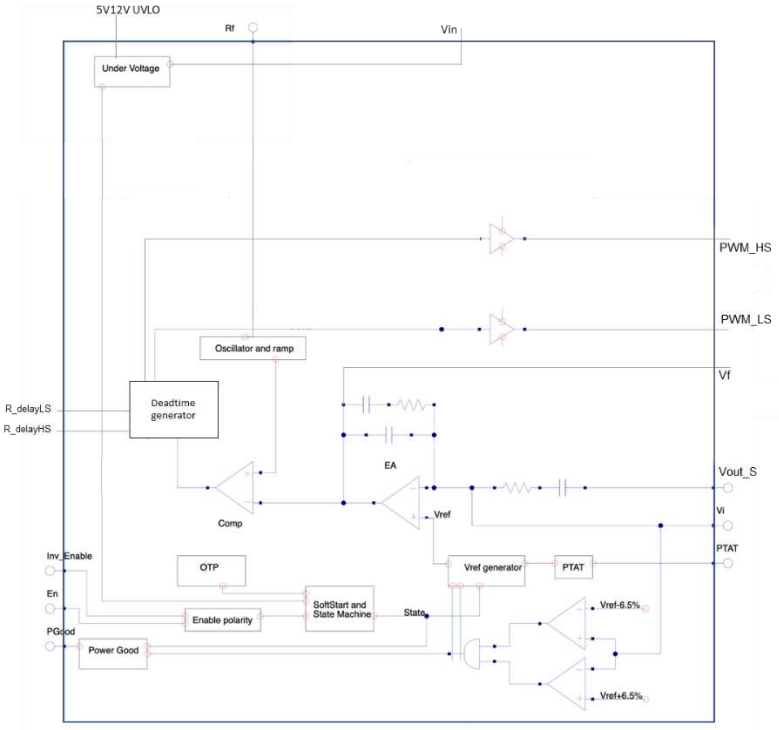


Figure 6: Control system block diagram.

Package description

EPCS4001 is packaged in a 32pin plastic Quad Flat No-Lead (QFN) package 5.0x5.0x0.9mm in size, with an exposed pad to be soldered to the PCB for better thermal properties.

Figure 7 shows the package dimensions and recommended footprint.

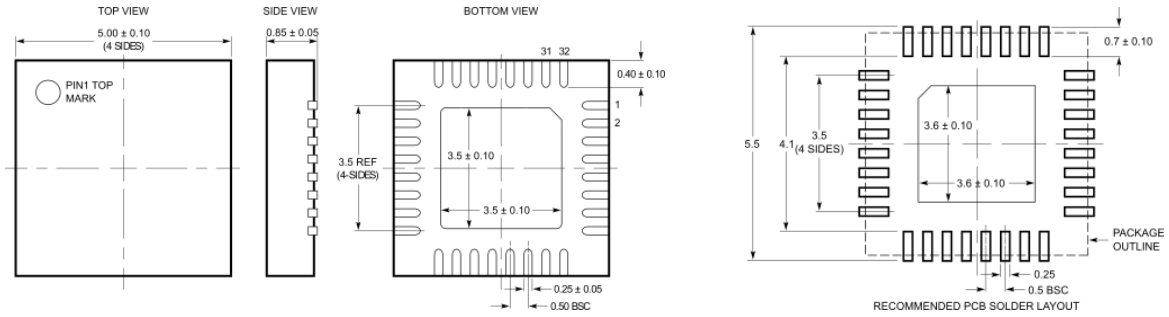


Figure 7: QFN32 package dimensions for the controller.

Design guidelines and operation

EPCS4001 is a half bridge buck converter controller explicitly designed to work with EPC7011 and EPC7009 power stages or drivers, in high radiation and magnetic field environments such as High Energy Physics experiments or space applications. EPCSC401 is the buck DC-DC converter composed by EPCS4001 and EPC7011.

Embedded linear regulators
EPCS4001 integrates all regulators required for powering the internal control electronics. Furthermore, two linear regulators LinPOL48V (48V-input) and LinPOL12V (12V-input) are integrated on-chip to supply logic power of the GaN power stage. All storage capacitors required for the internal control regulators are on-chip and have been sized to ensure steady voltage even during large current surges. LinPOL48V and LinPOL12V require 1uF and 1uF external ceramic capacitors, respectively, placed as close as possible to their output pins.

Linear regulators Under-Voltage lockout
The embedded linear regulators need sufficient headroom voltage to provide stable output to the control circuitry. To prevent faulty operation because of lack of appropriate supply, a comparator enables operation only when Vin_Ctrl is above 3.4V (rising). This comparator has a hysteresis, and the linear regulators are disabled again when Vin_Ctrl falls below 3.1V.

EPCS4001 controls Under-Voltage lockout and coordination with power stage
EPC7011 and EPC7009 have embedded VDD UVLOs and to ensure proper coordination, the controller enters in soft-start procedure only when Vin_Ctrl (which is normally connected to power stage/driver VDD) is above 10.5V in rising edge.
The comparator which is used to define this threshold has a hysteresis and the EPCS4001 is turned off when Vin_Ctrl falls below about 10V.

Enabling EPCS4001
The control circuitry is disabled by default by an internal 500 kΩ pull-down resistor on the EN pin; therefore it won't start unless the enable pin (EN) has not been asserted by a voltage above 0.8V. The Enable pin has a hysteresis of 300mV, therefore EPCS4001 will turn off when Enable pin's voltage falls below 0.5V.
The polarity of the enable signal can be inverted by connecting the Inv_Enable pin to GND. In this case, the circuit is disabled when a voltage above 0.8V is applied to the enable (EN) pin, and vice versa the circuit is enabled when a voltage below 0.5V is applied; notice that in this case, it is enabled by default if the EN pin is floating through the internal pull-down resistor of 500 kΩ.

Soft Start procedure
When EPCSC401 converter (EPCS4001 and EPC7011) is enabled, a large current is required to charge the output capacitors to the nominal regulated voltage. This current must be limited to safe levels. A pre-defined Soft Start (SS) procedure limits the inrush current by progressively increasing the reference voltage of the Error Amplifier (EA). The output voltage reaches the nominal value in about 400us when using 2MHz switching frequency and 250us for 3MHz switching frequency. Every time the controller is disabled – either by acting on the En pin, by under-voltage lockout, or by OTP detection – it follows the same sequence to reach the state where it regulates the nominal output voltage. This sequence is managed through an embedded state machine. Soft start ends when the rising reference voltage slightly exceeds the bandgap reference voltage. The reference to the EA is then switched to the steady reference generator (bandgap). It is hence normal to observe a small overshoot in Vout at the end of the SS procedure.

Power Good flag
The PG output pin is used to signal that EPCS4001 is correctly regulating the output voltage. For easy compatibility with almost any CMOS logic level up to 3.3V, this is an open drain output. This transistor is normally off when the controller is regulating correctly, while it is turned on in any other state. In the absence of Vin, or in under-voltage lockout, power is not provided to the control electronics and the open-drain transistor cannot exert its pull-down function. To avoid PG rising in this condition, it is recommended to use the buck converter output as pull-up voltage (via a voltage divider, to guarantee maximum 3.3V). Current in the NMOS open drain transistor must be limited to 500uA, while the absolute maximum voltage on the PG pin is 3.3V.

Over-Temperature Protection (OTP)
A dedicated circuit monitors the controller junction temperature and disables EPCS4001 when it reaches about 120ºC. The OTP has a hysteresis of about 40ºC, hence the controller restarts (with SS) when the junction temperature decreases below 80ºC.

Compensation network
The compensation network is fully integrated and determines a typical loop bandwidth of about 100kHz in the recommended operation conditions (frequency, voltage ranges, inductor, on-board passives). EPCS4001 is hence capable of quickly adjusting the output voltage in case of output load transients.

Cooling
EPCS4001 contains a linear regulator which could dissipate a large amount of power depending on the load. VDD of EPC7011 could require up to 30mA, which produces a power dissipation in the order of 1.5W for 48V input voltage and 12V output. The QFN32 package has an exposed cooling pad to which the IC is directly attached. This pad must be soldered to the GND plane of the PCB with sufficient thermal dissipation capability in order to maintain a suitable junction temperature.

Proportional To Absolute Temperature (PTAT) voltage

The PTAT analog signal can be used to monitor the temperature (T) rise of the EPCS4001 ASIC during operation, to verify that the cooling is appropriate. The absolute value of the PTAT voltage at a given T can have a wide sample-to-sample variability. However, the PTAT rise rate with respect to T is very close to a straight line with a 8.5 mV/ºC slope. This linear dependence is shown in Figure 8 in a nominal case. The discontinuity above 100ºC is due to the OTP trip and a hysteresis being added to the overtemperature protection. Given the variability in the absolute value of the PTAT, it is possible to observe low-end saturation at 0V and variable offset with respect to temperature at which the output rises above 0V.

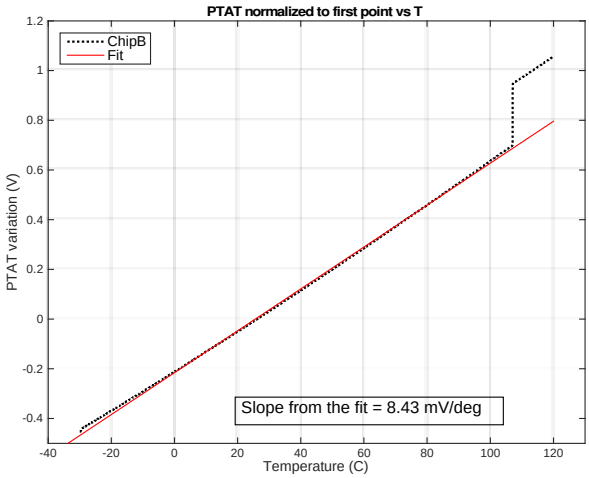


Figure 8: PTAT voltage vs Temperature.

DC-DC converter design guidelines

This section presents the guidelines for the design of the rad-hard buck converter (EPCSC401). The PCB design files are available, and it is strongly recommended to re-use them as much as possible, as they represent the output of an optimal design and ensure stability, performance and long-term reliability of both the controller and the GaN Power Stage.

Figure 9 shows the block diagram of EPCSC401. The most relevant design criteria of each block will be described in this section.

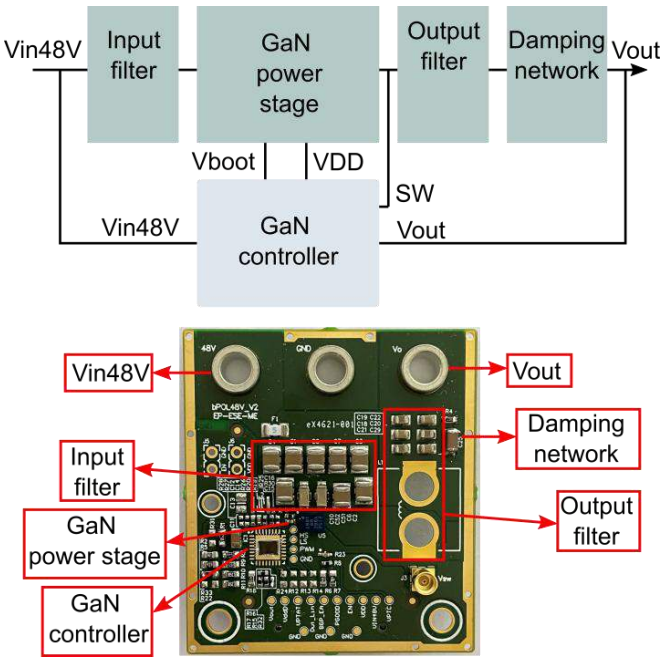


Figure 9: EPCSC401 block diagram (top) and PCB (bot)

Input filter and GaN power stage

The input filter serves two purposes: input voltage and current ripple reduction, and voltage stress reduction on the power devices. The input power loop in a Buck converter is shown on Fig. 10, it is formed by the loop between the input capacitors Cin and power switches Sw1 and Sw2. This loop presents a trapezoidal-shaped current with fast edges that, in combination with the parasitic inductances highlighted in red, could create high amplitude voltage transients and oscillations.

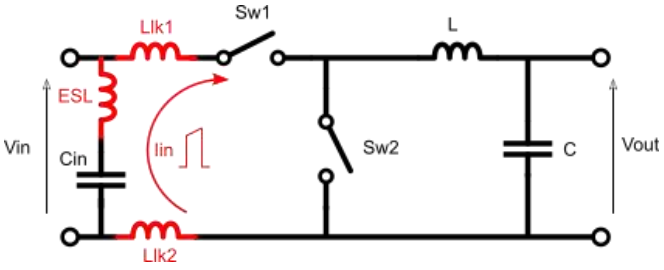


Figure 10: Input power loop parasitic inductances.

To have reliable operation, the parasitic inductances of the board and packages (Llk1 and Llk2) and the ESL of the input capacitors should be reduced as much as possible.

The ESL reduction can be achieved by the proper selection of the technology and packages of the capacitors. For EPCSC401, a combination of high value bulk capacitors for ripple reduction and high frequency capacitors is required. For the bulk capacitance, using several 2.2uF 100V-rated ceramic capacitors is recommended. For the high frequency filtering, low ESL capacitors such as Murata NFM31KC104R2A3L should be placed as close as possible to the input power pins of the GaN power stage.

The reduction of the board parasitic inductance is achieved by generating a vertical power loop and reducing as much as possible the distance between the top and internal layers, as shown in Fig. 11. The recommended dielectric thickness between top and the first internal is 100um.

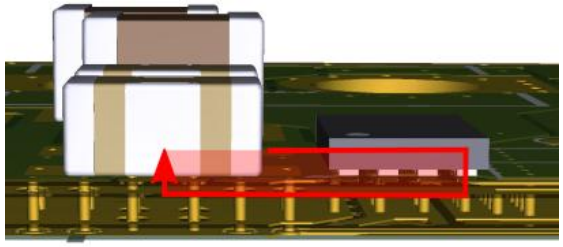


Figure 11: High frequency power loop.

Furthermore, the return GND path on the first internal layer (Layer 1) should be a solid uninterrupted plane. Therefore, if mechanical through-hole vias are used, it may be necessary to remove the unused pads to meet minimum trace width between vias, as shown in Fig. 12.

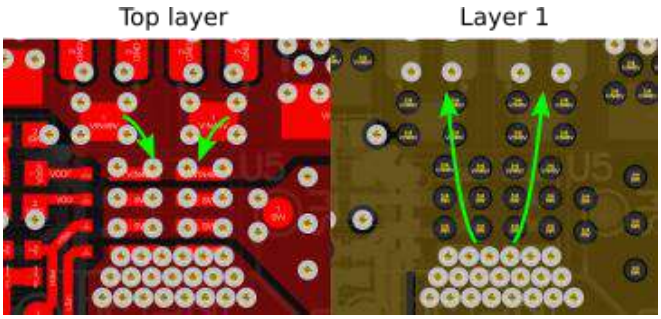


Figure 12: Power planes recommendation.

By following the above recommendations, the input power loop inductance is in the range of 150pH. This value has been obtained by both finite element analysis of the physical printed circuit board and experimental measurements.

Output filter and damping network

The output filter consists of a filter inductor and capacitors. The filter inductor defines the current ripple amplitude in combination with the switching frequency, input and output voltages, and it has a direct impact on the system efficiency. EPCSC401 has been tested and optimized for two configurations: one using a 220nH air core inductor for High Energy Physics applications, where the converter must operate in a high magnetic field environment, and the other using a 1uH ferromagnetic inductor for applications without magnetic field restrictions.

Moreover, given that the resonance between the inductor and filter capacitors could produce instabilities in the voltage control loop,

a RC damping network is recommended at the output, to reduce the resonance peak and avoid oscillations in the output voltage.

The table below shows the recommended value of the output filter components and switching frequency (fsw) for each configuration, where L is the value of the filter inductor; Cout is value, type and quantity of capacitors in parallel for the output filter capacitor; Rdamp is the value of the damping resistor and Cdamp is the value, type and quantity of capacitors in series with Rdamp. For stability reasons, the cutoff frequency of the LC filter should be between 30kHz and 50kHz, considering the real capacitance of Cout due to the dc bias of the ceramic capacitors.

The recommended fsw maximizes efficiency for the selected inductor value.

L	220nH	1uH
Cout	12x 22uF 25V 0805 MLCC	12x 10uF 25V 0805 MLCC
Rdamp	0.1Ω 0603	0.1Ω 0603
Cdamp	2x 47uF 16V 1210	2x 47uF 16V 1210
fsw	2MHz (Rf = 130kΩ)	1MHz (Rf = 270kΩ)

It is recommended to use as many capacitors in parallel as possible for Cout to minimize ESL, thus improving the filtering performance.

GaN controller and supply of GaN power stage

As previously described, the GaN controller integrates all linear regulators required to supply the internal electronics and the external GaN power stage from the 48V input voltage (Vin48V).

The output of LinPOL48V linear regulator (OUT_LIN) is internally connected to VDD12V pin through a diode. VDD12V is then used to supply the control electronics, via the VIN_CTRL pin, and the GaN power stage VDD. It is recommended to use an LC filter between VDD12V and VDD to eliminate possible transients produced by single event effects. The recommended values are 20nH (part number 0806SQ-19NGLC, if air core is required) and 22uF ceramic capacitor. Furthermore, for the VIN_CTRL input, a 100nF capacitor is recommended as close as possible to the pin.

As an added convenience to ensure a proper start of the converter, a fast diode has been integrated on the controller in order pre-charge the bootstrap capacitor. This diode may or may not be necessary if the power stage / driver already provides an integrated version. If in use, please follow the recommendations described in the “pin function” section for pin 26 (DiodeK).

Additional layout recommendations

EPCS4001 is available in a QFN-32 package with an exposed bottom pad. This pad should be soldered to the ground plane, using vias to provide good thermal transfer to the bottom side of the board. Using 17 filled and capped vias, 0.35mm hole diameter, spaced 1mm in the horizontal axis and 0.7mm in the vertical, with an interleaved arrangement yields approximately a thermal resistance of 10 ºC/W for the linear regulator (from PTAT measurement to bottom plate temperature).

It is recommended to use the second layer as a ground plane. The signal ground (controller) and the power ground should be connected on a single point, preferably at the logic input pins of the GaN power stage. This recommendation is aimed to prevent ground voltage bouncing on the controller due to the high magnitude current ripple in the power stage.

Typical waveforms and characteristics

Switching characteristics

Figure 13 shows the switching node voltage characteristics for two different load conditions, when using the recommended PCB layout. When Iout = 5A the inductor current is negative at the turn off of the low-side GaN FET, which causes the high-side GaN FET to conduct in reverse during the dead time. The reverse conduction voltage in this condition adds to the switching node voltage above the Vin value. When Iout = 10A, the converter operates with hard switching in all transistors.

As shown in Figure 13, there are no overvoltage spikes due to the optimization of the switching speed of the EPC7011 GaN power stage and the PCB layout.

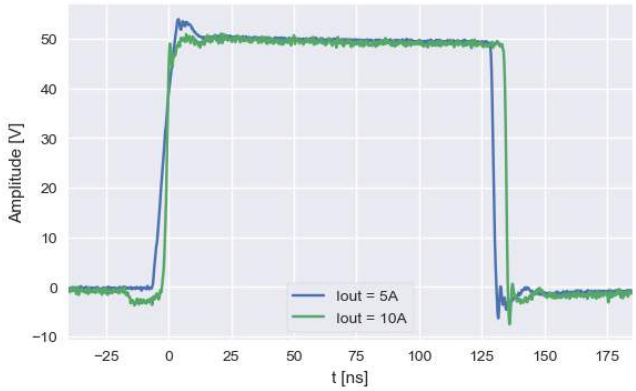


Figure 13: Switching node waveforms.
220nH inductor, 48Vin, 2MHz.

Efficiency

Efficiency for 220nH air core inductor, 12V output

The 220nH air core inductor has been built using Litz Wire (1125 x 0,071mm P155 from Elektrisola, total section 4.45mm^2) on a toroidal plastic core. This inductor is a custom design for the prototype, and design details are available upon request.

Figure 14: EPCSC401 with air-core 220nH inductor.

EPCSC401 has been tested for different input voltages in the recommended configuration, detailed in the design guidelines section, up to Iout = 13A. The cooling of the converter has been performed from the bottom of the PCB, with a cooling plate temperature between 20 ºC and 30ºC.

The obtained efficiency is shown in Fig. 15. It should be noted that, depending on the load and input voltage, the converter operates with the high side switch in zero voltage turn-on or hard turn-on. The change in the operating mode is indicated with different markers on the figure.

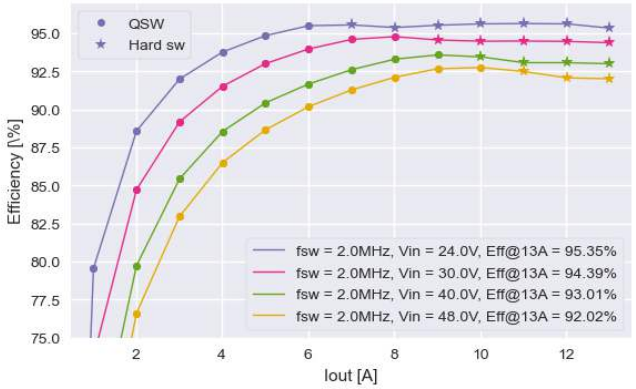


Figure 15: Efficiency, 220nH air-core inductor.

Efficiency for 1uH ferromagnetic core inductor, 12V output

For the case of the 1uH ferromagnetic inductor, the resulting efficiency is shown in Fig. 16 for different input voltage values and load condition up to 13A, using the recommended configuration in the design guidelines section.

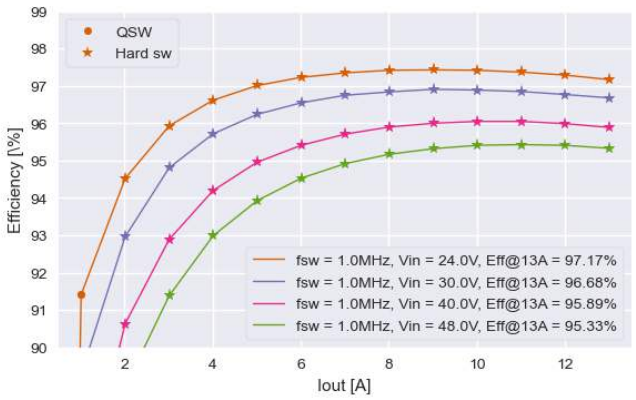


Figure 16: Efficiency, 1uH ferromagnetic core inductor.

Efficiency for 220nH ferrite core inductor, 1.9V output

For the case of the 220nH ferrite inductor, the resulting efficiency with fsw=1MHz is shown in Fig. 17 for different input voltage values and load condition up to 5A. Notice the excellent performance despite the high step-down ratio.

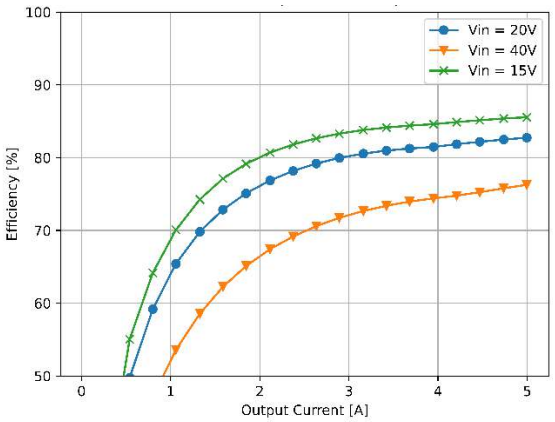


Figure 17: Efficiency, 220nH ferrite core inductor, 1MHz switching frequency.

Efficiency for 460nH air core inductor, 2.5V output

In this configuration, the EPCSC401 has been tested for the load conditions of the first stage of point of load converters: Vout=2.5V and up to 5A load current. The tested input voltages are 12V, 20V and 24V.
The figure below shows the picture of EPCSC401 using a toroidal air core inductor. The size of the board could be significantly reduced if this power level is required by reducing the number and footprint of the input and output capacitors, which, in this prototype, are rated to a higher voltage and sized to filter larger current ripples.

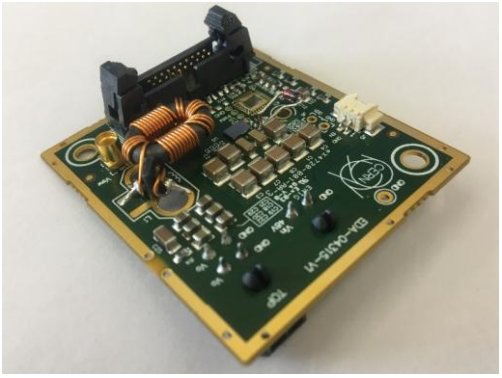


Figure 18. EPCSC401 using the FEASTMP inductor.

Figure 19 shows the efficiency when using this configuration and fsw=2MHz. As shown, the converter is suitable to be used for Vin up to 24V. The minimum input voltage is 12V, to ensure the correct voltage supply for the EPC7011 logic and driving stages.

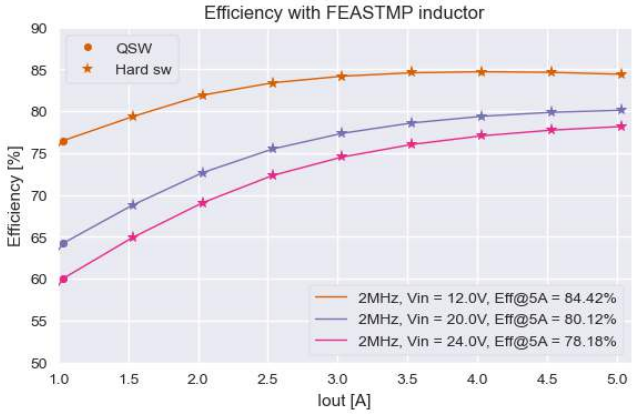


Figure 19. Efficiency of EPCSC401 with 460nH small air-core inductor and Vout=2.5V.

Line and Load regulation

Figures 20 and 21 show the EPCSC401 performance with respect to steady state line and load regulation.

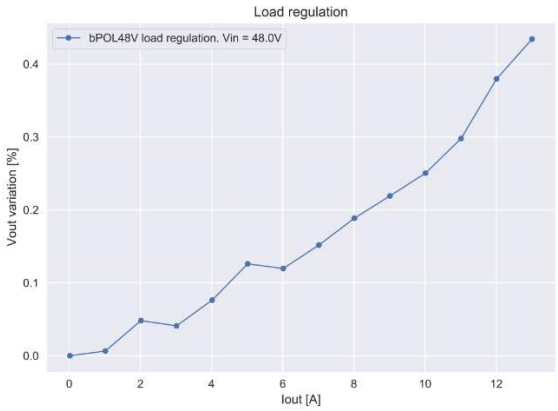


Figure 20. EPCSC401 Load regulation characteristic

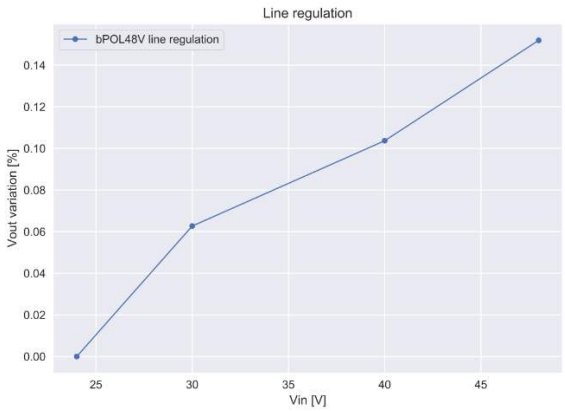


Figure 21. EPCSC401 Line regulation characteristic

Radiation tolerance

TID – Total Ionizing Dose

EPCSC401 with the 220nH inductor configuration has been irradiated with x-rays to study the TID effects, using the X-ray irradiation system at CERN. This system is the Seifert RP149, part of the CERN-EP-ESE equipment, which is routinely used for TID tests of deep submicron technologies. With a 50kV-3kW tube, a tungsten target and a 150µm thin Al filter, it produces an X-ray spectrum that has been well characterized in literature and is well accepted by the industry.

Figure 22 and Figure 23 show output voltage vs TID when testing at room temperature and at -30ºC, respectively. Both figures have two horizontal axes, the top one indicating the dose deposited on the GaN powerstage and the bottom one indicates the dose on the Si controller. The test at room temperature was conducted up to a TID of 228 Mrad for the controller and 432 MRad for the GaN power stage. There is no significant change in the output voltage due to radiation up to the tested dose. All other variables such as internal regulators, PTAT signal, bandgap and efficiency are also stable and close to pre-rad specifications up to the reached TID.

The test at -30ºC was conducted up to a TID of 67 Mrad for the controller and 126 MRad for the GaN power stage. The temperature control was done on the coldplate in which the converter is mounted, so the actual temperature on the controller and power stage is larger. Similarly to the ambient temperature test, there is no significant change in the output voltage due to radiation up to the tested dose. All other variables such as internal regulators, PTAT signal, bandgap and efficiency are also stable and close to pre-rad specifications up to the reached TID.

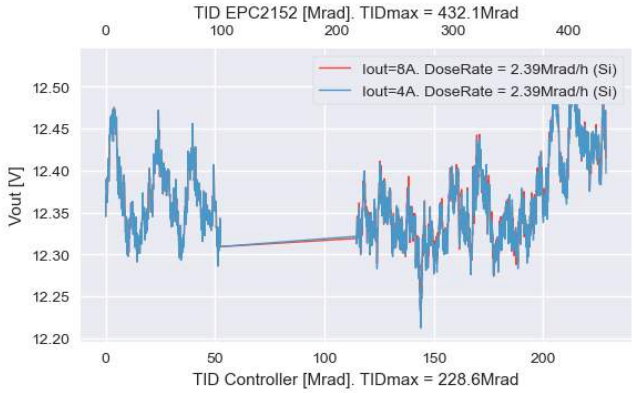


Figure 22. EPCSC401 Vout vs TID. Ambient temperature.
Note: Acquisition failed between 52MRad and 114MRad

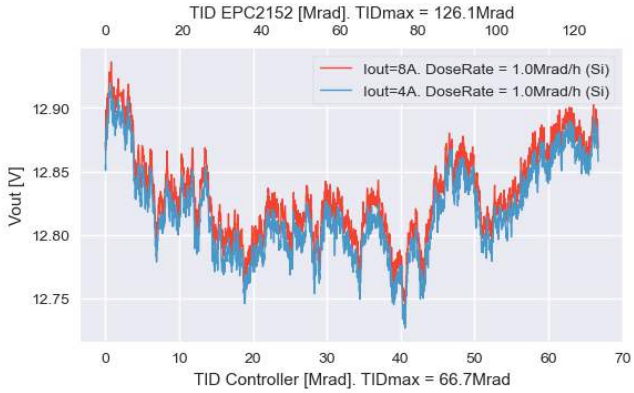


Figure 23. EPCSC401 Vout vs TID. -30ºC temperature.

SEE - Single Event Effects

The single event effects (SEE) have been evaluated for the controller using heavy ions on the EPCSC401 in the Cyclotron Resource Center of UC Louvain. In these tests, the effect on the GaN power stage is negligible, as the range of the heavy ions is not large enough to deposit charge on the sensitive area of the device. The GaN power stage is also fully characterized by EPC Space.

Figure 24 shows the single event induced Vout transients for different linear energy transfers (LET). The transients have been categorized in two types depending on the sign of the variation with respect to the average value: Type-0 when the transients are negative, and Type-1 when the transients are positive. An example of the shape of these transients is shown on the right-hand side of the figure. The left-hand side of the figure shows the distribution of the amplitude (in absolute value), for each LET. The horizontal axis label also shows the number of events and the reached fluence for each case.

The ions and tilt angles corresponding to each of the tested LETs are listed on the table below.

Ion	Tilt angle [degrees]	Equivalent LET (Si) [MeV/(mg/cm²)]
$^{36}Ar^{11+}$	0	9.9
$^{36}Ar^{11+}$	45	14
$^{58}Ni^{18+}$	0	20.4
$^{103}Rh^{11+}$	0	46.1
$^{103}Rh^{11+}$	45	65.2
$^{124}Xe^{35+}$	0	62.5
$^{124}Xe^{35+}$	45	88.4

EPCSC401 was tested up to LET = 88.4 MeV/(mg/cm²); no destructive events have been observed. In general, the amplitude of the transients increases with increasing LET. The maximum amplitude is around 25% for the Type-0 events, in rare cases and for LET > 62.5 MeV/(mg/cm²).

For High Energy Physics (HEP) applications, where statistically most of the events have LET<15 MeV/(mg/cm²), the maximum negative transient amplitude (Type-0) is below 10% and there are no positive events (Type-1).

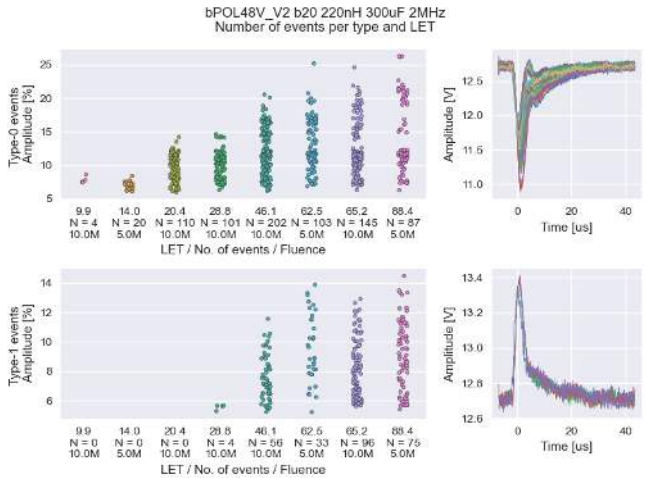


Figure 24. Single Event Transients

DD -Displacement Damage

For displacement damage (DD), the controller has been tested with 25MeV protons in the MC40 Cyclotron Facility in Birmingham and Neutrons in the TRIGA reactor in Ljubljana. There is no degradation for fluences up to 2.23E14 p/cm^2 and 4E14 n/cm^2.

For the case of the EPC GaN power stage, it has been irradiated with 24GeV protons in the IRRAD facilities at CERN and neutrons in the TRIGA reactor in Ljubljana. There is no degradation for fluences up to 2.5E15 p/cm^2 and 1E15 n/cm^2.

Revision history

Revision	Date	Description
0	April 2025	First document release