LSI/CSI = LS7866

LSI Computer Systems, Inc. 1235 Walt Whitman Road, Melville, NY 11747 (631) 271-0400

32-BIT QUADRATURE COUNTER WITH I²C INTERFACE

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GENERAL FEATURES:
- Operating voltage: 3V to 5.5V
- Up to 30MHz count frequency
- Dual Mode-registers for functional programmability
- Dual 32-bit comparators
- Dual 32-bit Input Data registers for dual target counts
- 32-bit latch for counter upload
- Dual Status registers for dynamic and freeze-frame status
- Quadrature A, B and Z inputs with digital filters.
- Programmable quadrature or non-quadrature input modes
- 8-bit, 16-bit, 24-bit or 32-bit programmable configurations
- Up to 400 KHz I²C clock speed
- 3 selectable address pins for up to 8 devices on the bus
- Write-All addressing mode for writing to all devices simultaneously
- 14-pin SOIC and TSSOP packages

PIN ASSIGNMENT
TOP VIEW

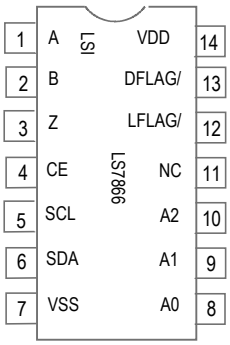

Fig 1

GENERAL DESCRIPTION:
LS7866 is a monolithic CMOS 32-bit counter, programmable to operate in 8-bit, 16-bit, 24-bit or 32-bit modular structures. Inputs are provided to interface directly with the quadrature clocks and the index markers from incremental encoders. The programmable modes include: X1/X2/X4 quadrature or bi-directional non-quadrature. Either of these modes can further be combined with Free-Run, Non-Recycle, Mod-N and Range-Limit modes. The functional modes are programmed via two control registers: MCR0 and MCR1. An I²C standard serial bus in 7-bit address format is provided for communicating with the LS7866.

IO PINS:
A (pin 1), B (pin 2). Inputs.
In quadrature mode A and B clocks from incremental encoders are directly applied to the A and B inputs. These clocks are ideally 90° out of phase signals. A and B inputs are digitally filtered for noise suppression and decoded for count clocks and up/down direction. With A leading B count UP is selected, with A lagging B count DOWN is selected. In non-quadrature mode A serves as the count input (counter advances at the falling edge) and B as the up/down direction control input with B=1 selecting UP and B=0 selecting DOWN count modes. In non-quadrature mode A and B inputs are not filtered but reshaped with input Schmitt trigger buffers.

Z (pin 3). Input.
Z is a programmable input to function as one of the following:

- LCI0: Load CNTR with IDR0
- LCI1: Load CNTR with IDR1
- RCNT: Reset CNTR
- RDST: Reset DSTR
- LSST: Load SSTR with DSTR
- LODC: Load ODR with CNTR
- LODC-RCNT: LODC at negative edge and RCNT at positive edge

The Z input is programmable to be either edge sensitive or level sensitive. With the exception of LODC-RCNT configuration, in the edge sensitive mode a high to low transition causes the intended event to occur. In the LODC-RCNT configuration each edge performs a different function. In level sensitive mode a logic low is the active level. In the quadrature mode, Z input is digitally filtered with the same internal clock used for validating A and B inputs. In non-quadrature mode the Z input is not filtered.

CE (pin 4). Input.
Count Enable input. A high at the CE input causes the A and B inputs to be enabled while a low, causes them to be disabled. The CE input has an internal pull-up.

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SCL (pin 5). Input.
Clock input for synchronizing the serial data on the SDA bus. Since the LS7866 can operate in the slave mode alone, the SCL clocks must be provided by a bus master.

SDA (pin 6). Input/Output.
All bi-directional serial data transfer between the LS7866 and the bus master takes place over the SDA bus in accordance to standard I^2C protocol. As an input, high level noise immunity is obtained with a combination of built-in Schmitt trigger and digital filter circuits. As an output the SDA bus is an open drain FET driver requiring an external pull-up to +V supply rail.

VSS (pin 7).
Power Supply negative terminal or GND

A0 (pin 8), A1 (pin 9), A2 (pin 10). Inputs.
Address inputs. These inputs constitute the 3 low order address bits of the standard I^2C 7-bit address field. The 7-bit device address is formed by appending the 3 low order address bits to the 4 high order fixed address bits designated as: 1110 (Note1). The complete device address is therefore, $1110A_2A_1A_0$. An exception to this format is the Write-All format: 0000xxx, where the address bits xxx are ignored. In the Write-All addressing mode all devices on the bus are simultaneously enabled and written into.

(Note1. Special order parts with different fixed address in the range of 0001 to 1111 is available)

LFLAG/ (pin 12). Output.
The LFLAG/ is a programmable output for signaling one or all of the following events:
• CY (CARRY: indicates CNTR overflow)
• BW (BORROW: indicates CNTR underflow)
• EQL0 (indicates CNTR = IDR0). (See note *)
• EQL1 (indicates CNTR = IDR1). (See note **)
• INDEX (indicates Z input in active state)

LFLAG/ output is programmed via FCR. The LFLAG/ output switches low on becoming active and remains low until cleared by a reset DSTR command. LFLAG/ is an open drain output allowing multiple device LFLAG/ outputs to be connected in wire-OR configuration with a single pull-up resistor to form a single interrupt for the host processor.
(* In Range-Limit mode EQL0 occurs in down count mode only).
(** In Range-Limit, Non-Recycle and Modulo-n modes EQL1 occurs and EQL1TGL toggles in up count mode only)

DFLAG/ (pin 13). Output.
The DFLAG/ is a programmable output for signaling one or all of the following events:
• CY (CARRY: indicates CNTR overflow)
• BW (BORROW: indicates CNTR underflow)
• EQL0 (indicates CNTR = IDR0). (See note *)
• EQL1 (indicates CNTR = IDR1). (See note **)
• INDEX (indicates Z input in active state)
• EQL1TGL (toggles at each occurrence of EQL1). (See note **)
• BWTGL (toggles at each occurrence of BW)
• UD (indicates count direction: UP = 1, DOWN = 0)

The DFLAG/ output is programmed via FCR to produce a “low” output pulse dynamically for the selected event.
(* In Range-Limit mode EQL0 occurs in down count mode only).
(** In Range-Limit, Non-Recycle and Modulo-n modes EQL1 occurs and EQL1TGL toggles in up count mode only)

VDD (pin 14). Power Supply positive terminal.

REGISTERS:
There are several internal registers for data and control functions. The registers are accessible for read and write over the SDA bus. In a master-initiated communication sequence, the first byte holds the device address; the second byte holds the register address according to table 1.

Table1

ADDRESS (R7..R0)	REGISTER	RD	WR
000d 0000	MCR0	yes	yes
000d 0001	MCR1	yes	yes
000d 0010	FCR	yes	yes
000d 0011	IDR0	yes	yes
000d 0100	IDR1	yes	yes
000d 0101	TPR	no	yes
000d 0110	ODR	yes	no
000d 0111	CNTR	yes	no
000d 1000	SSTR	yes	no

•R[7:5] = 000 fixed.
•R[4] = d = 0: R[3:0] bits are used as absolute register address without auto increment. For read/write to a multi-byte register, the successive bytes are sequentially read or written, from most to least significant byte positions automatically.
•R[4] = d = 1: R[3:0] bits are used as absolute address with auto address increment mode enabled. In auto address increment mode a register address is needed to be sent only once in a communication sequence. Once the addressed register has been accessed for read or write, successive bytes are read or written into successive registers in incremental addresses. In RD operation TPR address is skipped and address rolls over to 0001 0000 going past 0001 1000. In WR operation address rolls over to 0001 0000 going past 0001 0101.

MCR0. The mode control register MCR0 must be initialized after power up to configure the following functional modes:

MCR0

B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

B[1:0] = 00: non-quadrature count mode.
(A = count clock, B = up/down control)
= 01: X1 quadrature count mode. (1 count per quad)
= 10: X2 quadrature count mode. (2 count per quad)
= 11: X4 quadrature count mode. (4 count per quad)
B[3:2] = 00: free-running count mode.
= 01: Non-Recycle count mode.
= 10: Range-Limit count mode.
= 11: Modulo-n count mode.
B[6:4] = 000: disable Z input
= 001: configure Z as LCI0 input. (CNTR <= IDR0).
= 010: configure Z as LCI1 input. (CNTR <= IDR1).
= 011: configure Z as RCNT input. (reset CNTR).
= 100: configure Z as RDST input. (reset DSTR).

(MCR0 contd.)
B[6:4] = 101: configure Z as LSST input. (SSTR <= DSTR).
= 110: configure Z as LODC input. (ODR <= CNTR). ***
= 111: configure Z as both RCNT and LODC input.
In this mode Z input is edge sensitive; high-to-low transition performs LODC function and low-to-high transition performs RCNT function. This configuration overrides B[7] setting.
B[7] = 0: Z input is high to low edge-sensitive.
= 1: Z input is low-active level-sensitive.
At power-up the MCR0 is cleared to 0.

*** A LODC (ODR <= CNTR) operation is always accompanied by a LSST (SSTR <= DSTR) operation

Definitions of count modes.
• Non-Recycle mode: CNTR freezes at CNTR = IDR1+1 with generation of EQL1 in up and at CNTR = -1 with generation of BW in down count modes. Counting re-enabled with Load CNTR or Reset CNTR.
• Range-Limit mode: Up and Down count ranges are limited between IDR1 (high) and IDR0 (low) respectively. CNTR freezes at these limits resuming counting when the direction reverses.
• Modulo-n: input count clock frequency fc is divided by a factor of (n+1) in both up and down directions, where n = IDR1. The resultant frequency, fo = fc/(n+1) is made available at the FLAG/ output when FCR register bits B[1] and B[3] are set to 1. A frequency of fo = fc/[2*(n+1)] results at the FLAG/ output when the FCR register bits B[5] and B[6] are set to 1.

MCR1. The mode control register MCR1 controls the following functional modes:

MCR1

B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

B[1:0] = 00: 4-byte mode (Affects IDR0, IDR1, ODR, CNTR).
= 01: 3-byte mode (Affects IDR0, IDR1, ODR, CNTR).
= 10: 2-byte mode (Affects IDR0, IDR1, ODR, CNTR).
= 11: 1-byte mode (Affects IDR0, IDR1, ODR, CNTR).
B[2] = 0: enable counting
= 1: disable counting
B[5:3] = No function
B[6] = 0: do not reset DSTR when CNTR is read.
= 1: reset DSTR when CNTR is read.
B[7] = 0: load SSTR with DSTR when CNTR is read.
= 1: do not load SSTR with DSTR when CNTR is read.

(With B[6] = 1 and B[7] = 0, a RD_CNTR operation also simultaneously uploads DSTR into SSTR followed by a reset of DSTR). At power-up the MCR1 is cleared to 0.

FCR. The flag control register FCR enables or disables the signals which can be produced at the DFLAG/ output and/or set the LFLAG/ output latch.

FCR

B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

B[0] = 1: enable CY. CY is generated when CNTR overflows.
B[1] = 1: enable BW. BW is generated when CNTR underflows.
B[2] = 1: enable EQL0. EQL0 is generated at CNTR = IDR0.

(FCR contd.)
B[3] = 1: enable EQL1. EQL1 is generated at CNTR = IDR1.
B[4] = 1: enable IDX. IDX is generated whenever Z input is in active state.
B[5] = 1: enable EQL1TGL. EQL1TGL signal toggles between high and low, for every occurrence of CNTR = IDR1 in up count mode only. B[5] is forced to 0 when B[7] = 1.
B[6] = 1: enable BWTGL. BWTGL signal toggles between "high" and "low", for every occurrence of borrow (BW). B[6] is forced to 0 when B[7] = 1.
B[7] = 1: enable count direction. 0 and 1 at the DFLAG/ output indicate DOWN and UP count modes respectively. B[7] = 1 forces all other FCR bits to 0.

DFLAG/ output is affected by all FCR bits. In contrast LFLAG/ output is affected by FCR bits B[0] through B[4] only.

When B[5] = 1 or B[6] = 1 or B[7] = 1, B[0] through B[4] functions are disabled. When a bit is set to 0, the corresponding function is disabled on the DFLAG/ and LFLAF/ outputs. At power-up the FCR is reset to 0.

TPR. The TPR is a virtual register which when written into generates transient signals for performing tasks such as transferring data between registers and clearing registers.

TPR

B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

B[0] = 1: RCNT: Reset CNTR (CNTR <= 0).
(B[0] = 1 overrides B[1], B[2] and B[6])
B[1] = 1: LCI0: Load CNTR with IDR0 (CNTR <= IDR0).
B[2] = 1: LCI1: Load CNTR with IDR1 (CNTR <= IDR1).
(B[1] and B[2] must not be high simultaneously)
B[3] = 1: LODC: Load ODR with CNTR (ODR <= CNTR).
B[4] = 1: LSST: Load SSTR with DSTR (SSTR <= DSTR).
B[5] = 1: RDST: Reset DSTR (DSTR <= 0) and LFLAG/
B[6] = 1: No function
B[7] = 1: MRST: Resets IDR0, IDR1, CNTR, ODR, DSTR, SSTR and LFLAG/.
(MRST overrides B[1] through B[4] and B[6].)

Data written into TPR are not stored, thereby releasing the referenced registers for normal operation following a write to TPR.

DSTR. The dynamic status register DSTR stores the count related instantaneous status.

DSTR

B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

B[0] = PLS: Power Loss. PLS = 1 indicates that a power down occurred since the last DSTR reset.
B[1] = CE: Count Enabled. CE = 1 indicates counting is enabled.
B[2] = IDX: Index. IDX = 1 indicates that Z input was in the active state since the last DSTR reset.
B[3] = EQL0. EQL0 = 1 indicates that CNTR = IDR0 condition occurred since the last DSTR reset.
B[4] = EQL1. EQL1 = 1 indicates that CNTR = IDR1 condition occurred since the last DSTR reset.

(DSTR contd.)
B[5] = BW: Borrow. BW = 1 indicates that a CNTR underflow occurred since the last DSTR reset.
B[6] = CY: Carry. CY = 1 indicates that a CNTR overflow occurred since the last DSTR reset.
B[7] = UD: Up/Down. UD = 1 indicates count up and UD = 0 Indicates count down directions.
An instantaneous snap-shot of the DSTR can be stored in the SSTR and read back on the SDA bus. A functional configuration can also be made with MCR1 for auto transfer of DSTR to SSTR whenever the CNTR is read. This guarantees the proper correlation between the CNTR data and DSTR data whenever the CNTR is read. At power-up DSTR is reset to 0.

SSTR. The static status register, SSTR holds the count related status information with bit mapping identical to the DSTR register.

SSTR

B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

B[0]=PLS: Set to one upon power up." Power loss" indicator.
B[1]=CE: High indicates "counting enabled".
B[2]=IDX: High indicates Z input in active state.
B[3]=EQL0 : High indicates CNTR = IDR0.
B[4]=EQL1: High indicates CNTR = IDR1.
B[5]=BW: High indicates CNTR underflow
B[6]=CY: High indicates CNTR overflow
B[7]=UD: High indicates count up, low indicates count down

The instantaneous state of DSTR can be stored in SSTR either under event control such as the Z input (see MCR0) or under program control with a LSST command (see TPR). A functional configuration can also be made with MCR1 for auto transfer of DSTR to SSTR whenever the CNTR is read. This guarantees the proper correlation between the CNTR data and DSTR data whenever the CNTR is read. (Note: An LSST command is automatically executed along with the LODC command)

At power-up SSTR is reset to 0.

IDR0. The input data register, IDR0 is a 32-bit read/write register.

IDR0

B[31:24]	B[23:26]	B[15:8]	B[7:0]
Byte3	Byte2	Byte1	Byte0

The IDR0 can be uploaded into the CNTR for presetting the CNTR. IDR0 serve as the CNTR lower limit in range-limit count mode (see MCR0). IDR0 is scalable to operate in 1 to 4-byte modes (see MCR1). At power-up IDR0 is reset to 0.

IDR1. The input data register, IDR1 is a 32-bit read/write register.

IDR1

B[31:24]	B[23:26	B[15:8]	B[7:0]
Byte3	Byte2	Byte1	Byte0

The IDR1 can be uploaded into the CNTR for pre-setting the CNTR. IDR1 may also serve as CNTR upper limit in Range-Limit and Non-Recycle count modes (see MCR0). In Mod-n count mode IDR1 holds the count division factor n (see MCR0). IDR1 is scalable to operate in 1 to 4-byte modes (see MCR1).

ODR. The output data register, ODR is a 32-bit read only register. The ODR can be used as a repository for the CNTR.

ODR

B[31:24]	B[23:16]	B[15:8]	B[7:0]
Byte3	Byte2	Byte1	Byte0.

The instantaneous value of the CNTR can be stored in the ODR either under event control such as, the active level at the Z input (see MCR0 configuration) or under program control with a LDC_ODR command (see TPR). A transfer of CNTR to ODR under either event control or program control also causes an auto transfer of DSTR to SSTR in order to maintain the proper correlation between the count data and the status register. ODR is scalable to operate in 1 to 4-byte modes (see MCR1).

At power-up ODR is reset to 0.

CNTR. The CNTR is a 32-bit up/down counter programmable to operate in several different modes. It can be programmed to

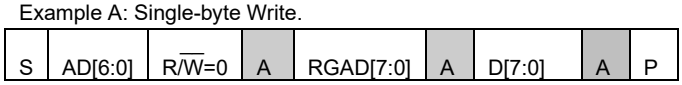
CNTR

B[31:24]	B[23:16]	B[15:8]	B[7:0]
Byte3	Byte2	Byte1	Byte0

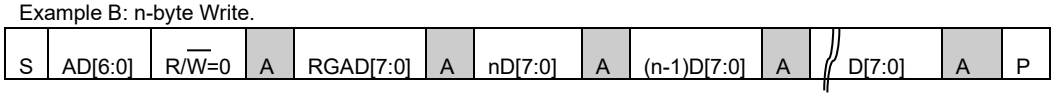
operate as either quadrature counter or non-quadrature counter. In either mode it can be configured further into Free-Running, Non-Recycle, Range-Limit or Mod-n modes (see MCR0). The CNTR can be preset with data from IDR0 and IDR1. IDR0 and IDR1 also set the data boundaries for the CNTR in special count modes such as, Non-Recycle, Range-Limit and Mod-n. Instantaneous CNTR value can be stored in the ODR for later retrieval. The CNTR can be read directly on the SDA bus. The CNTR is scalable to operate in 1 to 4-byte modes (see MCR1).

Samples of data transmission formats on the SDA bus..

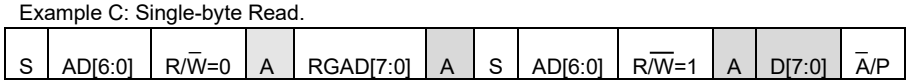
Example A: Single-byte Write.



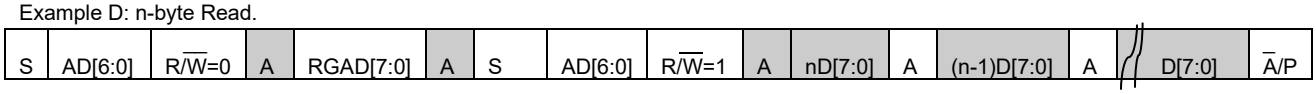
Example B: n-byte Write.



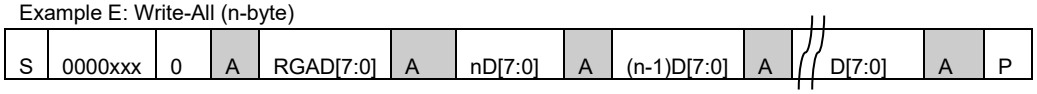
Example C: Single-byte Read.



Example D: n-byte Read.



Example E: Write-All (n-byte)



Glossary:

Sent by master

Sent by slave

♦S: Start bit; first bit sent by master signaling the start of a communication sequence.

♦AD[6:0]: 7-bit device address in the format $1110A_2A_1A_0$, where bits 1110 are fixed and $A_2A_1A_0$ constitute device addresses ranging between 0 and 7. Received bits $A_2A_1A_0$ are compared to address pins A2, A1 and A0 of a device. When matched, the device is enabled for communication. In Write-All communications AD[6:0] is fixed at 0000xxx, where x= don't care.

♦R/$\overline{W}$: Read or Write. R/$\overline{W}$ = 0 causes a write while R/$\overline{W}$ = 1 causes a read. In Write-All communication R/$\overline{W}$ must be a 0.

♦A: Acknowledge bit sent by the receiving device (master or slave) to acknowledge the successful receipt of a byte.

♦RGAD[7:0]: Register address in the format $000dR_3R_2R_1R_0$ (see table1) where $R_3R_2R_1R_0$ is in the range of 0000 to 1000.

- d = 0 causes read/write to a single register selected by address $R_3R_2R_1R_0$ according to table1.The single register read/write may be of the format of examples A or C when the addressed register is a single byte register, such as, MCR0, MCR1 etc. The single byte read/write may also be of the format of examples B or D when the addressed register is a multi-byte register, such as, IDR0, CNTR etc.
- d = 1 causes read/write to multiple registers starting with the register addressed by $R_3R_2R_1R_0$. After the completion of read/write to one register (either single or multi-byte), the address is auto incremented for accessing the next register in the address sequence. When addressing a multi-byte register, the address is incremented only after the completion of read/write of all the bytes for that register. In READ operation the address for TPR is skipped in the increment sequence and $R_3R_2R_1R_0$ rolls over to 0000 going past the address 1000. In the WRITE operation $R_3R_2R_1R_0$ rolls over to 0000 going past the address 0101.

♦D[7:0]: Data byte for read or write. In multi-byte communications the bytes are ordered from most-significant-byte to least-significant-byte, thus n representing the most-significant-byte in examples B and D.

♦$\overline{A}$: Not-Acknowledge bit. ♦P: STOP bit.
Either $\overline{A}$ or P sent by the master terminates a communication cycle requiring a new S bit for starting a new cycle.

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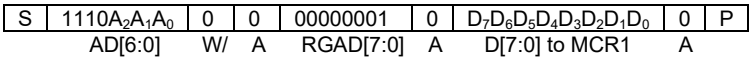
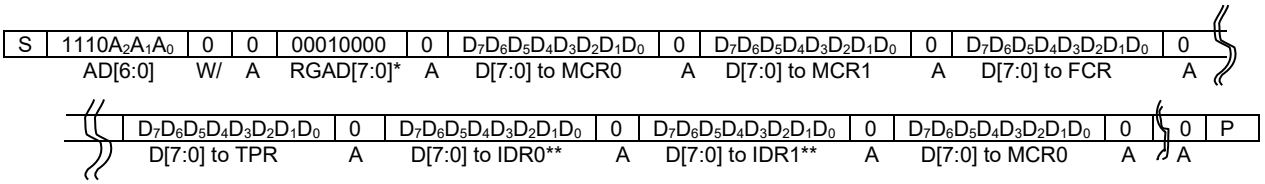
Note1. During a READ cycle if a transmitted logic high from one device conflicts with a logic low from another device on the bus, the high transmitting device aborts transmission by relinquishing the bus until being addressed with a new START.

Note2. A START bit inserted anywhere in a communication cycle aborts the cycle and starts a new communication cycle. A STOP bit inserted anywhere in a communication cycle aborts the cycle. The START and STOP bits however, can only be inserted when the SDA bus is not held low by the transmitting device.

Examples:

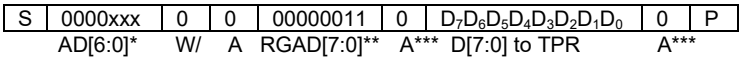


Example 1: Write to MCR1



* Auto address increment starting with MCR0 address
** Shown here is 1-byte mode. In 2-byte, 3-byte and 4-byte modes the register address is incremented only after the relevant number of bytes have been written into IDR0 or IDR1.

Example 2: Write to multiple registers with auto address increment



* Write-All address mode. All devices on the bus are enabled for write. xxx= don't care.
** Register TPR is selected in all devices for write
*** Every device on the bus sends back acknowledge A.

Example 3. Write-All to TPR

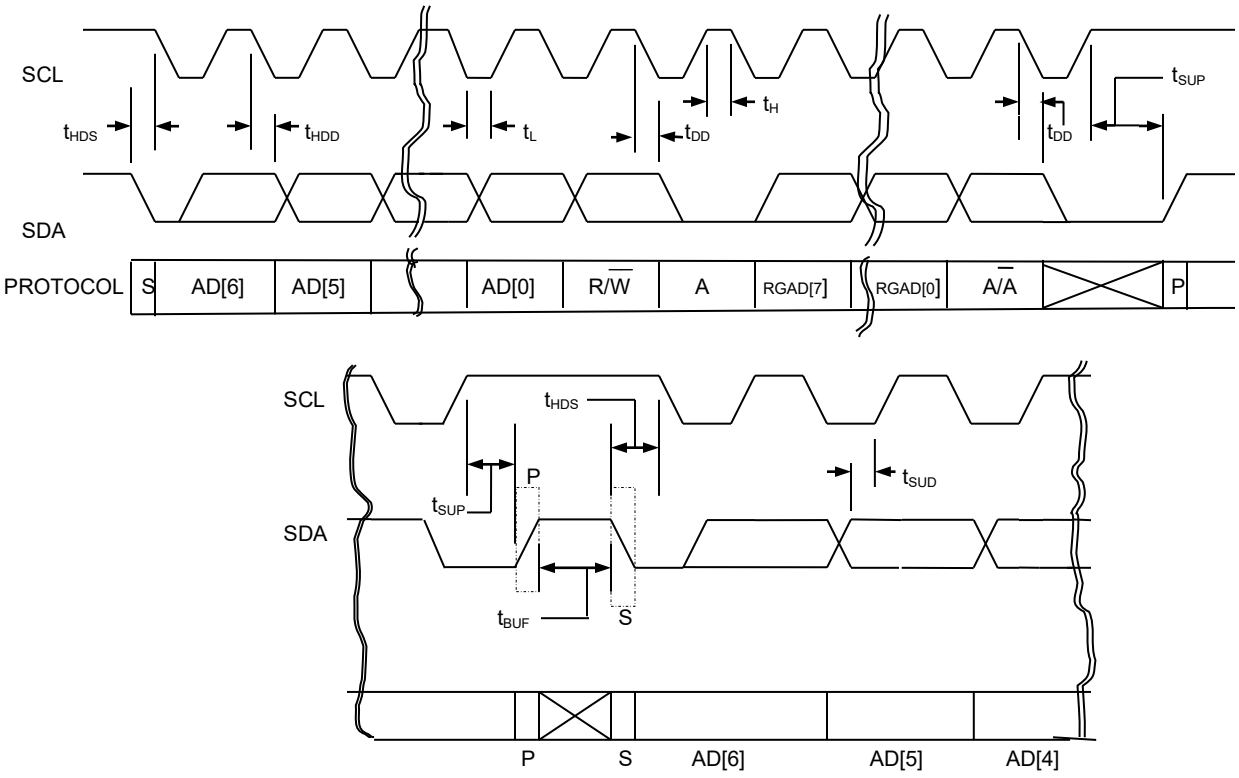


Fig 2. I²C Transient Parameters

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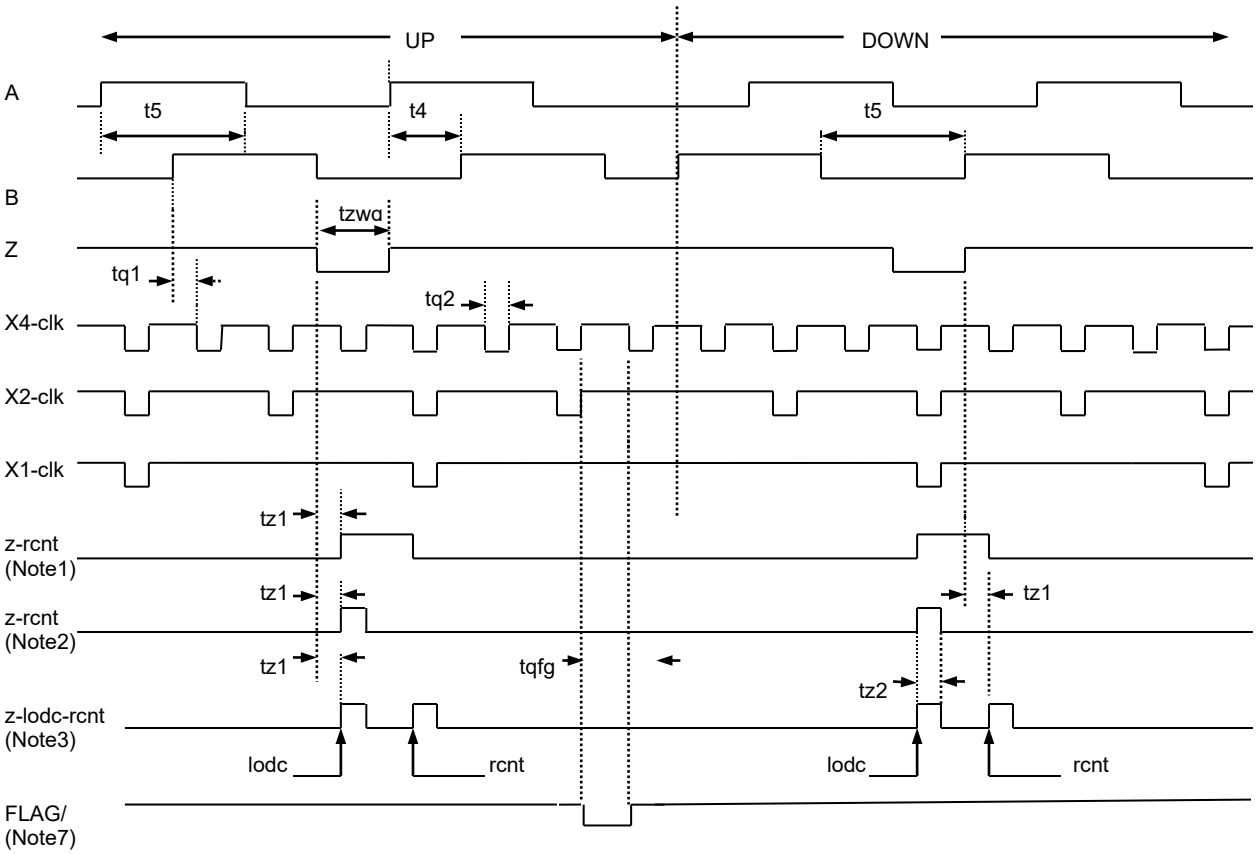

Note1. Internal RCNT signal from Z input when the Z input is configured for RCNT function in the level sensitive mode.
Note2. Internal RCNT signal from Z input when the Z input is configured for RCNT function in the edge sensitive mode.
Note3. Internal LODC and RCNT signals from Z input when the Z input is configured for LODC-RCNT function.
Note4. x1-clk, x2-clk and x4-clk are internal count clocks in x1 and x2 and x4 modes.
Note5. Z is not required to be synchronous with A or B to be a valid signal. It may occur in any phase relationship with respect to A and B.
Note6. CNTR advances on the falling edge of x1 or x2 or x4 clk.
Note7. FLAG/ output for Carry or Borrow in pulse mode (shown in x4 mode)

Fig 3. A, B and Z inputs in quadrature count mod

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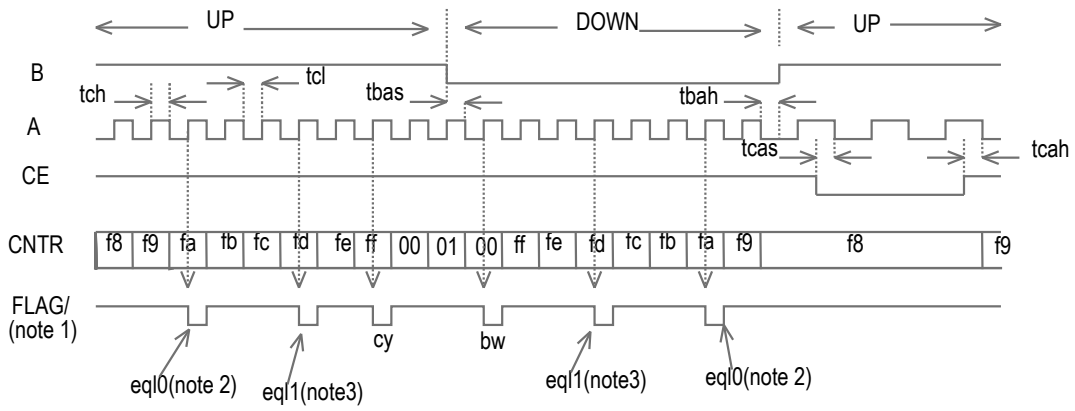
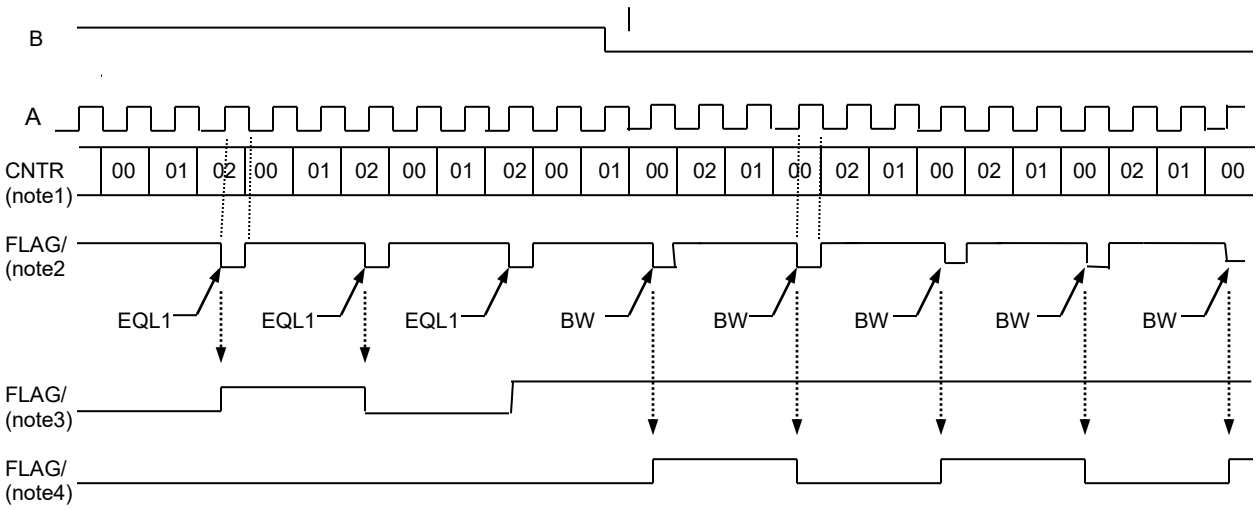


Note1. FLAG/ configured to output EQL0, EQL1, CY and BW in PULSE mode
Note2. In Range-Limit mode EQL0 is generated in DOWN count direction only
Note3. In Range-Limit, Non-Recycle and Modulo-n modes EQL1 is generated in UP count direction only
Note4. Shown in 1-byte configuration with IDR0 and IDR1 arbitrarily chosen to be fa and fd and CNTR starting at f8.

Fig 4. A, B, CE and FLAG/ in non-quadrature mode



Note1. IDR1 is assumed to be set to 02 (n = 02) causing a divide-by-3 modulo-n count scale
Note2. FLAG/ is configured to output EQL1 and BW in PULSE mode
Note3. FLAG/ is configured to output EQL1TGL
Note4. FLAG/ is configured to output BWTGL

Fig 5. Modulo-n, non-quadrature mode

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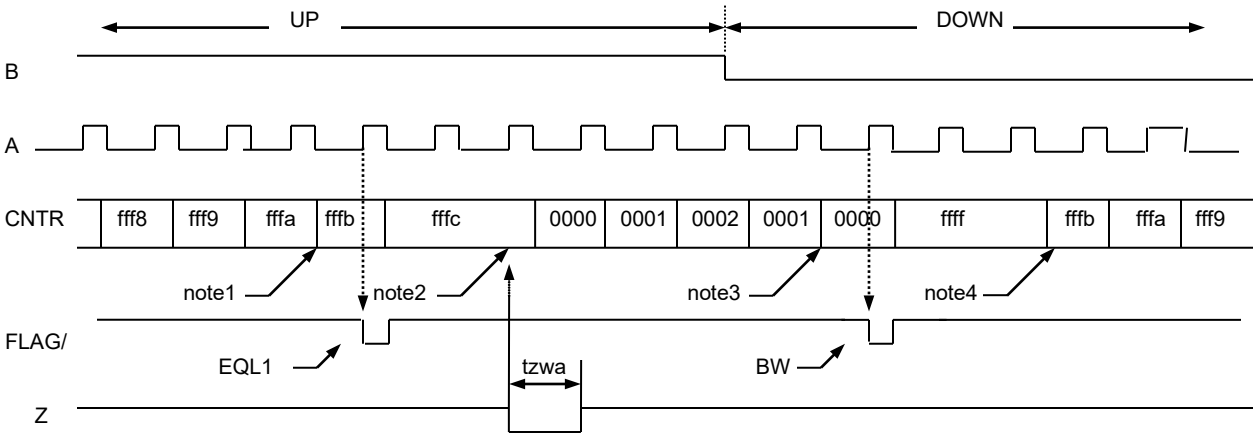
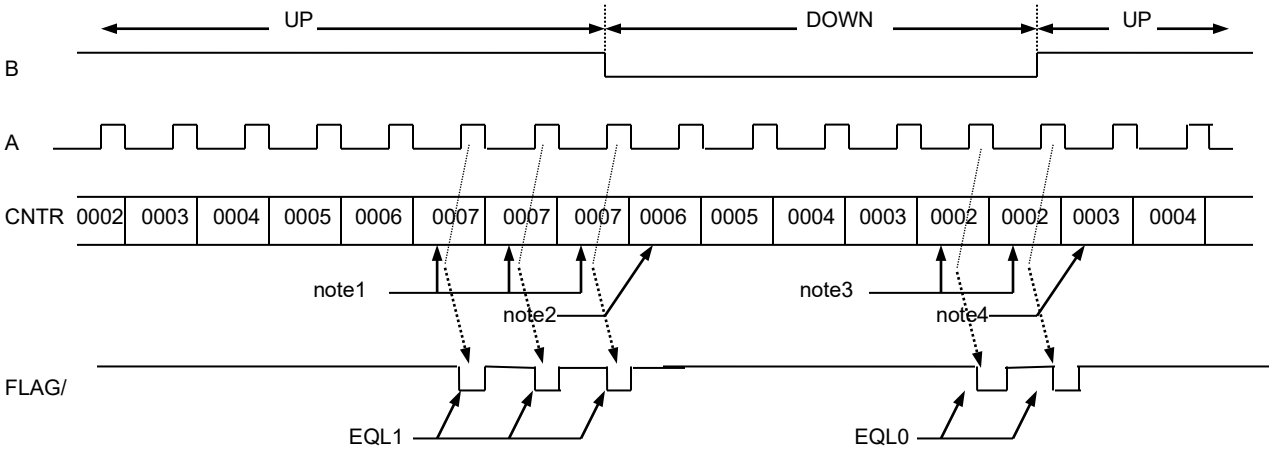


Note1. CNTR disabled at CNTR = IDR1 (set to fffb in 2-byte mode) with generation of a single EQL1 on the FLAG/ output and freezes at fffc.
Note2. CNTR re-enabled with a RCNTR operation via the Z input.
Note3. CNTR disabled at CNTR = 0000 with generation of a single BW on the FLAG/ output and freezes at ffff.
Note4. CNTR re-enabled with a load CNTR operation (LD1_CNTR in example).
Note5. FLAG/ configured to output EQL1 and BW in PULSE mode

Fig 6. Non-Recycle, non-quadrature mode



Note1. In UP direction CNTR freezes at CNTR = IDR1 (set to 0007 in example) with repeated generation of EQL1.
Note2. CNTR re-enabled with direction reversal.
Note3. In DOWN direction CNTR freezes at CNTR = IDR0 (set to 0002 in example) with repeated generation of EQL0.
Note4. CNTR re-enabled with direction reversal.
Note5. FLAG/ configured to output EQL0 and EQL1 in PULSE mode

Fig 7. Range-Limit , non-quadrature mode

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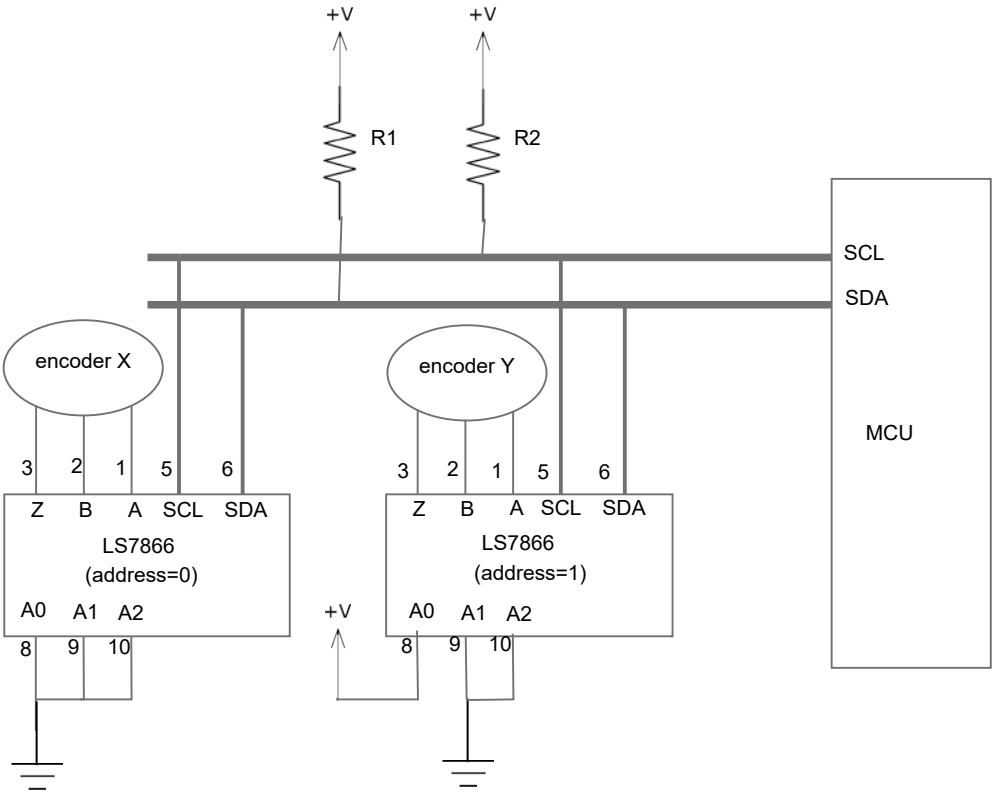
Absolute maximum ratings:			
Parameter	**Symbol**	**Value**	**Unit**
Supply Voltage	VDD	+7.0	Volts
Voltage at any input/output pin	Vin	VSS – 0.3 to VDD + 0.3	Volts
Operating temperature	Ta	-40 to +85	°C
Storage temperature	Ts	-65 to +150	°C

DC electrical characteristics: unless specified otherwise Ta = -25°C to +85°C, VDD = 5V						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**unit**	**Conditions**
Supply voltage	VDD	3.0	5.0	5.5	Volts	-
Supply current	IDD	-	1.2	1.8	mA	A, B, SCL, SDA held high or low; VDD = 5V
		-	500	750	uA	A, B, SCL, SDA held high or low; VDD = 3V
Logic low: A,B,Z,SCL,SDA	Vil	-	-	0.3*VDD		
Logic high: A,B,Z,SCL,SDA	Vih	0.7*VDD	-	-		
Logic low (all other inputs)	Vil	-	-	0.4*VDD	Volts	
Logic high (all other inputs)	Vih	0.6*VDD	-	-	Volts	
SDA output low	Volsda	-	-	0.5	Volts	Iolsda = 19mA
FLAG/ output low	Volflg	-	-	0.5	Volts	Iolflg = 5mA
FLAG/ output high	Vohflg	VDD – 0.5	-	-	Volts	Iohflg = -5mA
SDA output sink	Iolsda	19	25	-	mA	Volsda = 0.5, VDD = 5.0V
		12	16	-	mA	Volsda = 0.5, VDD = 3.0V
DFLAG/, LFLAG/ output sink	Iolflg	5	6	-	mA	Volflg = 0.5V, VDD = 5.0V
		3	4	-	mA	Volflg = 0.5V, VDD = 3.0V
DFLAG/ output source	Iohflg	- 3.3	- 4	-	mA	Vohflg = 4.5V, VDD = 5.0V
		- 1.8	- 2.5	-	mA	Vohflg = 2.5V, VDD = 3.0V
CE input low current	Ilce	-10	-15	-30	uA	Vi = 0.3*VDD, VDD = 3V to 5V
CE input high current	Ihce	1	-	4	uA	Vi = 0.7*VDD, VDD = 3V to 5V
All other inputs current	-	-	-	100	nA	Leakage current

Transient characteristics: unless specified otherwise Ta = -25°C to +85°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**unit**	**Conditions**
SCL clock frequency	**fscl**	-	-	**500**	**kHz**	**VDD = 5.0V**
		-	-	**375**	**kHz**	**VDD = 3.0V**
Bus idle time between STOP and START	**t_{BUF}**	-	**750**	-	**ns**	**VDD = 5.0V**
		-	**1000**		**ns**	**VDD = 3.0V**
SCL hold time for START	**t_{HDS}**	-	**250**	-	**ns**	**VDD = 5.0V**
		-	**330**	-	**ns**	**VDD = 3.0V**
SCL setup time for STOP	**t_{SUP}**	-	**250**	-	**ns**	**VDD = 5.0V**
		-	**330**	-	**ns**	**VDD = 3.0V**
SCL to SDA data out delay	**t_{DD}**	-	**500**	-	**ns**	**VDD = 5.0V**
		-	**660**		**ns**	**VDD = 3.0V**
SDA setup time	**t_{SUD}**	-	**250**	-	**ns**	**VDD = 5.0V**
		-	**330**		**ns**	**VDD = 3.0V**
SCL low duration	**t_L**	-	**1.0**	-	**us**	**VDD = 5.0V**
		-	**1.3**	-	**us**	**VDD = 3.0V**
SCL high duration	**t_H**	-	**1.0**	-	**us**	**VDD = 5.0V**
		-	**1.3**	-	**us**	**VDD = 3.0V**
Noise rejection by SCL and SDA input filters	-	-	-	300	ns	
Quadrature mode (fig 3):						
A to B to A separation	**t4**	**130**	-	-	**ns**	**VDD = 5.0V**
		200	-	-	**ns**	**VDD = 3.0V**
A, B pulse width	**t5**	**260**	-	-	**ns**	**VDD = 5.0V**
		400	-	-	**ns**	**VDD = 3.0V**
A, B frequency	**f_{QAB}**	-	-	**2.0**	**MHz**	**VDD = 5.0V**
		-	-	**1.3**	**MHz**	**VDD = 3.0V**
A or B to x1/x2/x4 count clock delay	**tq1**	-	**130**	**190**	**ns**	**VDD = 5.0V**
		-	**200**	**300**	**ns**	**VDD = 3.0V**
X1/x2/x4 count clock pulse width	**tq2**	-	**35**	-	**ns**	**VDD = 5.0V**
		-	**50**	-	**ns**	**VDD = 3.0V**

Quadrature mode (continued from previous page)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**unit**	**Conditions**
FLAG/ output pulse width for EQL0, EQL1	tqfg	-	t4 - 35	-	ns	x4, pulse mode, VDD = 5.0V
		-	t4 - 50	-	ns	X4, pulse mode, VDD = 3.0V
		-	2*t4 - 35	-	ns	X2, pulse mode, VDD = 5.0V
		-	2*t4 - 50	-	ns	X2, pulse mode, VDD = 3.0V
		-	4*t4 - 35	-	ns	X1, pulse mode, VDD = 5.0V
		-	4*t4 - 50	-	ns	X1, pulse mode, VDD = 3.0V
FLAG/ output pulse width for CY, BW	tqfg	-	t4 - 35	-	ns	x4, pulse mode, VDD = 5.0V
		-	t4 - 50	-	ns	X4, pulse mode, VDD = 3.0V
		-	2*t4 - 35	-	ns	X2, pulse mode, VDD = 5.0V
		-	2*t4 - 50	-	ns	X2, pulse mode, VDD = 3.0V
		-	4*t4 - 35	-	ns	X1, pulse mode, VDD = 5.0V
		-	4*t4 - 50	-	ns	X1, pulse mode, VDD = 3.0V
Z input high or low transition to z-lodc, z-rcnt pulse delay	tz1	250	-	380	ns	Edge sensitive and dual edge modes. VDD = 5.0V
		400	-	600	ns	Edge sensitive and dual edge modes. VDD = 3.0V
Z input pulse width	tzw	130	-	-	ns	VDD = 5.0V
		200	-	-	ns	VDD = 3.0V
Non-quadrature mode (fig 4):						
A input high	tch	25	-	-	ns	VDD = 5.0V, 27 deg C
		41	-	-	ns	VDD = 3.0V, 27 deg C
A input low	tcl	25	-	-	ns	VDD = 5.0V, 27 deg C
		41	-	-	ns	VDD = 3.0V, 27 deg C
A input frequency	f_A	-	-	20	MHz	VDD = 5.0V, 27 deg C
		-	-	12	MHz	VDD = 3.0V, 27 deg C
B input set up time	tbas	10	-	-	ns	VDD = 5.0V
		15	-	-	ns	VDD = 3.0V
B input hold time	tbah	10	-	-	ns	VDD = 5.0V
		15	-	-	ns	VDD = 3.0V
CE input set up time	tcas	10	-	-	ns	VDD = 5.0V
		15	-	-	ns	VDD = 3.0V
CE input hold time	tcah	10	-	-	ns	VDD = 5.0V
		15	-	-	ns	VDD = 3.0V
Z input pulse width	tzwn	15	-	-	ns	VDD = 5.0V, level sensitive mode
		20	-	-	ns	VDD = 3.0V, level sensitive mode
		130	-	-	ns	VDD = 5.0V, edge sensitive mode
		200	-	-	ns	VDD = 3.0V, edge sensitive mode
FLAG/ output pulse width for EQL0, EQL1	tnfg	-	tch	-	ns	-
FLAG/ output pulse width for CY, BW	tnfg	-	Tch	-	ns	-



R1 =/> 300Ω (based on SDA output sink capacity of LS7866)
R2 minimum is determined by the SCL output sink capacity of the MCU

Fig 8. Two axes quadrature counter with shared bus

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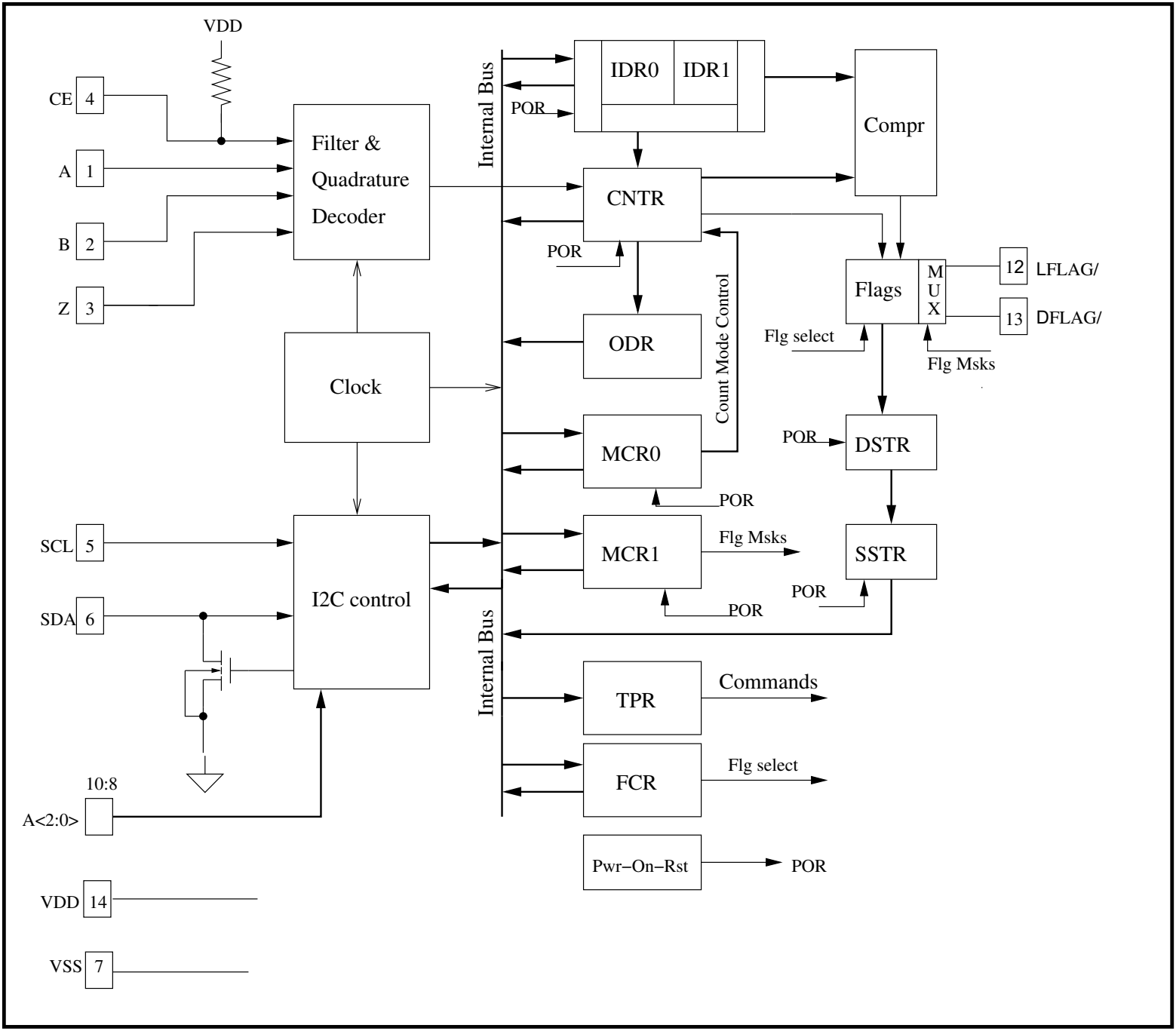

Fig 9. LS7866 block diagram