650V Half-Bridge GaNFast™ Power IC

Features

GaNFast power IC

- Two independent logic inputs with hysteresis
- Enable input
- Ultra-low standby current
- Wide V_{CC} range
- Low-side turn-on dV/dt slew rate control
- 200 V/ns dV/dt immunity
- ESD, high-side UVLO, shoot-through protection
- Floating high-side with internal level shift
- Integrated high-side bootstrap
- High-frequency operation up to 2 MHz

650V eMode GaN FETs

- 275 mΩ high-side FET
- 175 mΩ low-side FET
- Zero reverse recovery charge

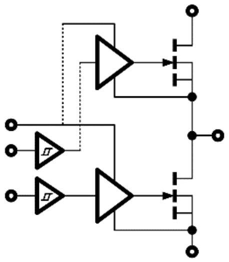
Small, low-profile SMT QFN

- 6x8 mm footprint
- 0.85 mm profile
- Minimized package inductance

Applications

- AC-DC
- DC-DC
- Active Clamp Flyback
- Buck
- Boost

PQFN 6x8 mm



Simplified Schematic

Description

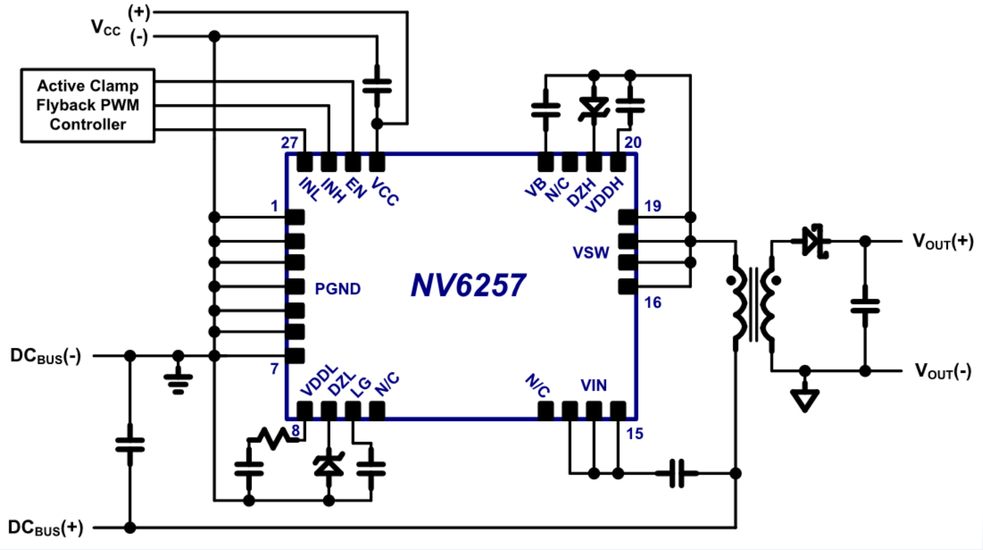
This GaN Power IC is a high performance, easy-to-use, 650V half-bridge GaNFast™ power IC, optimized for high-frequency, soft-switching topologies.

The feature-rich, monolithically-integrated GaNFast power IC with simple logic inputs, harnesses two high-performance eMode GaN FETs (275 mΩ high-side, 175 mΩ low-side) to create the fastest, smallest, most efficient powertrain in the world.

The highest dV/dt immunity, integrated protection features and industry-standard low-profile, low-inductance, 6x8 mm SMT QFN package combine to enable designers to exploit GaN technology with simple, quick, dependable solutions achieving breakthrough power density and efficiency.

Navitas' GaNFast power ICs extend the capabilities of traditional topologies such as flyback, half-bridge, buck/boost, resonant, etc. to MHz+ and enable the commercial introduction of breakthrough designs.

Typical Application Circuit: Active Clamp Flyback



Absolute Maximum Ratings (with respect to P_{GND} unless noted)

SYMBOL	PARAMETER	MAX	UNITS
V_{IN}	HV input	0 to +650	V
V_{SW}	Switch Node	-7 to +657	V
I_{OUTL} @ T_C=100ºC	Continuous output Current (Low-side FET)	8	A
I_{OUTL} PULSE@ T_C=25ºC	Pulsed output Current (Low-side FET)	14	A
I_{OUTH} @ T_C=100ºC	Continuous output Current (High-side FET)	5	A
I_{OUTH} PULSE@ T_C=25ºC	Pulsed output Current (High-side FET)	9	A
V_B (to V_{SW})	High-side gate driver bootstrap rail	30	V
V_{DDH} (to V_{SW})	High-side drive supply	7.2	V
DZ_H (to V_{SW})	High-side voltage regulator setting input	6.6	V
V_{DDL}	Low-side drive supply	7.2	V
DZ_L	Low-side voltage regulator setting input	6.6	V
EN	Enable input	30	V
IN_H, IN_L	High-/Low-side drive input	30	V
V_{CC}	Supply voltage	30	V
dV/dt	Slew Rate	200	V/ns
T_J	Operating Junction Temperature	-55 to 150	ºC
T_{STOR}	Storage Temperature	-55 to 150	ºC

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond absolute maximum ratings may cause permanent damage. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage	10	15	24	V
$V_{INH,L}$	High-/low-side drive input voltage	0	5	V_{CC}	V
DZ_L	Low-side drive set Zener voltage	5.8	6.2 (2)	6.6	V
DZ_H	High-side drive set Zener voltage	5.8	6.2 (2)	6.6	V

(2) Use of Zener diode other than 6.2 V is not recommended. See Table III for required 6.2 V Zener diode part numbers.

ESD Ratings

SYMBOL	PARAMETER	MAX	UNITS
HBM	Human Body Model (per JESD22-A114)	1000	V
CDM	Charged Device Model (per JESD22-C101F)	500	V

Thermal Resistance

SYMBOL	PARAMETER	TYP	UNITS
$R_{\theta JC}$ (2)	Junction-to-Case	1.8	ºC/W
$R_{\theta JA}$ (2)	Junction-to-Ambient	40	ºC/W

(2) R_{θ} measured on DUT mounted on 1 square inch 2oz Cu (FR4 PCB)

Electrical Characteristics

Typical conditions: V_{IN} = 400 V, V_{CC} = 15 V, F_{SW} = 1 MHz, T_{AMB} = 25 ºC, I_{OUT} = 1.5 A, $DZ_{L,H}$ = 6.2 V (unless otherwise specified)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
VCC Supply Characteristics						
V_{CCUV+}	V_{CC} UVLO Rising Turn-On Threshold		9.25		V	DZ_L = 6.2 V
V_{CCUV-}	V_{CC} UVLO Falling Turn-Off Threshold ($V_B – V_{SW}$)		8.75		V	DZ_L = 6.2 V
V_{CCUV_HYS}	V_{CC} UVLO Hysteresis		0.5		V	
I_{QCC_STBY}	V_{CC} Standby Current		130		µA	V_{CC} = 15 V, V_{IN} = 0 V, V_{EN} = 0 V, I_{SW} = 0 A
I_{QCC}	V_{CC} Quiescent Current		3.0		mA	V_{INH} = 0 V, V_{INL} = 0 V, V_{SW} = OPEN
I_{CC_SW}	V_{CC} Switching Current		10		mA	F_{SW} = 1 MHz
VDD Supply Characteristics						
V_{DDUV+}	V_{DD} UVLO Rising Turn-On Threshold		4.8		V	DZ_L = 6.2 V
V_{DDUV-}	V_{DD} UVLO Falling Turn-Off Threshold		4.5		V	DZ_L = 6.2 V
V_{DDUV_HYS}	V_{DD} UVLO Hysteresis		0.3		V	
Logic Inputs Characteristics						
$V_{INH,L+}$	Input Logic High Threshold (rising edge)			4	V	
$V_{INH,L-}$	Input Logic Low Threshold (falling edge)	1			V	
V_{I-HYS}	Input Logic Hysteresis		0.5		V	
t_{INHPLH}	Prop Delay (IN_H from Low to High, V_{SW} pulled to V_{IN})		45		ns	Fig 1
t_{INHPHL}	Prop Delay (IN_H from High to Low, V_{SW} tri-stated)		45		ns	Fig 2
t_{INLPLH}	Prop Delay (IN_L from Low to High, V_{SW} pulled to P_{GND})		15		ns	Fig 3
t_{INLPHL}	Prop Delay (IN_L from High to Low, V_{SW} tri-stated)		15		ns	Fig 4

Electrical Characteristics (cont.)

Typical conditions: V_{IN} = 400 V, V_{CC} = 15 V, F_{SW} = 1 MHz, T_{AMB} = 25 ºC, I_{OUT} = 1.5 A, $DZ_{L,H}$ = 6.2 V (unless otherwise specified)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
VB Supply Characteristics						
VB_{UV+}	V_B UVLO Rising Turn-On Threshold ($V_B – V_{SW}$)		9.0		V	DZ_H = 6.2 V
VB_{UV-}	V_B UVLO Falling Turn-Off Threshold ($V_B – V_{SW}$)		8.5		V	DZ_H = 6.2 V
VB_{HYS}	V_B UVLO Hysteresis		0.5		V	
I_{QVB}	V_B Quiescent Current		3		mA	V_{INH} = 0 V, V_{INL} = 0 V, V_{SW} = 0 V, V_B = 12 V, D_{ZH} = 6.2 V
Switching Characteristics						
F_{SW}	Switching Frequency			2	MHz	
t_{PW}	Pulse width	0.02		100	us	High side, no low side min
Bootstrap FET Characteristics						
I_{BOOT}	Bootstrap Charging Current		350		mA	V_{CC} = 12 V, V_B = 0 V, V_{SW} = 0 V
Enable Input Characteristics						
V_{EN+}	IC Enable Rising Turn-on Threshold			4	V	
V_{EN-}	IC Enable Falling Turn-off Threshold	1			V	
V_{EN_HYS}	IC Enable Hysteresis		0.5		V	

Electrical Characteristics (cont.)

Typical conditions: V_{IN} = 400 V, V_{CC} = 15 V, F_{SW} = 1 MHz, T_{AMB} = 25 ºC, I_{OUT} = 1.5 A, $DZ_{L,H}$ = 6.2 V (unless otherwise specified)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
High-side GaN FET Characteristics						
$R_{DS(ON)}$	High-side FET Drain-Source Resistance		350		mΩ	V_{INL} = 6 V, V_{INH} = 0 V, I_D = 2.5 A
V_{SD}	Source-Drain Reverse Voltage		3.5	5	V	V_{INL} = 0 V, V_{INH} = 0 V, I_{SD} = 2.5 A
Q_{OSS}	Output Charge		13		nC	V_{DS} = 400V, V_{INL} = 0 V, V_{INH} = 0 V
Q_{RR}	Reverse Recovery Charge		0		nC	V_{DS} = 400 V
C_{OSS}	Output Capacitance		13		pF	V_{DS} = 400V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(er)}^{(1)}$	Effective Output Capacitance, Energy Related		20		pF	V_{DS} = 400 V V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(tr)}^{(2)}$	Effective Output Capacitance, Time Related		33		pF	V_{DS} = 400 V V_{INL}=0 V, V_{INH} = 0 V
Low-side GaN FET Characteristics						
$R_{DS(ON)}$	Low-side FET Drain-Source Resistance		180		mΩ	V_{INL} = 0 V, V_{INH} = 6 V, I_D = 4 A
V_{SD}	Source-Drain Reverse Voltage		3.5	5	V	V_{INL} = 0 V, V_{INH} = 0 V, I_{SD} = 4 A
Q_{OSS}	Output Charge		20		nC	V_{DS} = 400 V V_{INL} = 0V, V_{INH} = 0 V
Q_{RR}	Reverse Recovery Charge		0		nC	V_{DS} = 400 V
C_{OSS}	Output Capacitance		20		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(er)}^{(1)}$	Effective Output Capacitance, Energy Related		31		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(tr)}^{(2)}$	Effective Output Capacitance, Time Related		50		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V

Note 1: $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400V

Note 2: $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400V

Electrical Characteristics (cont.)

Propagation Delay Definition

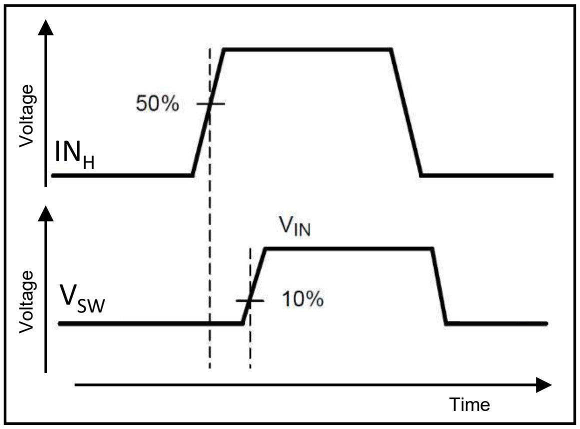


Fig 1: Propagation Delay Buck Mode t_{INHPLH}

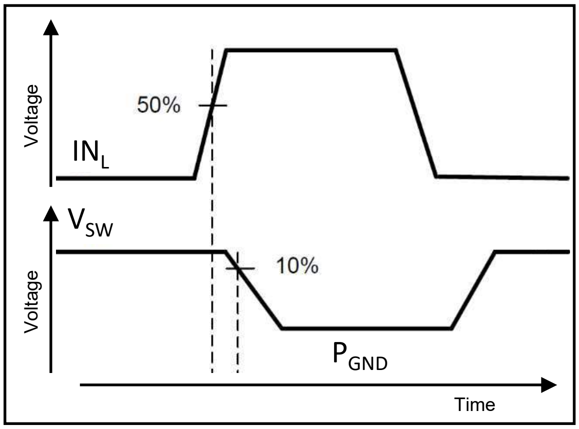


Fig 2: Propagation Delay Boost Mode t_{INHPHL}

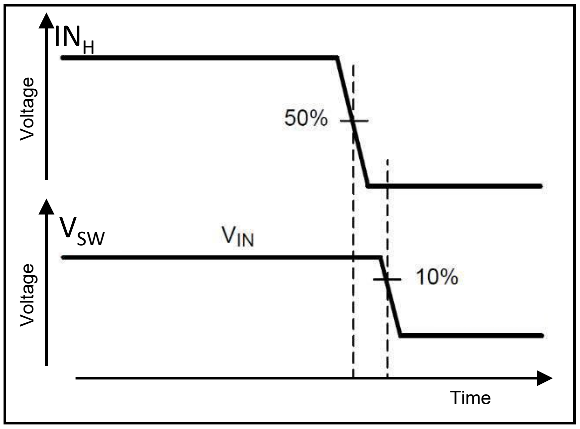


Fig 3: Propagation Delay Buck Mode t_{INLPLH}

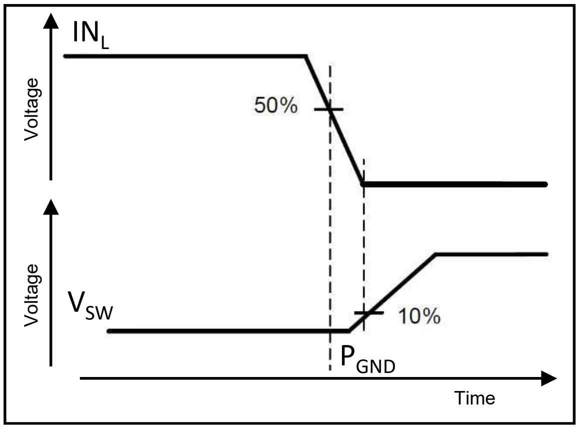
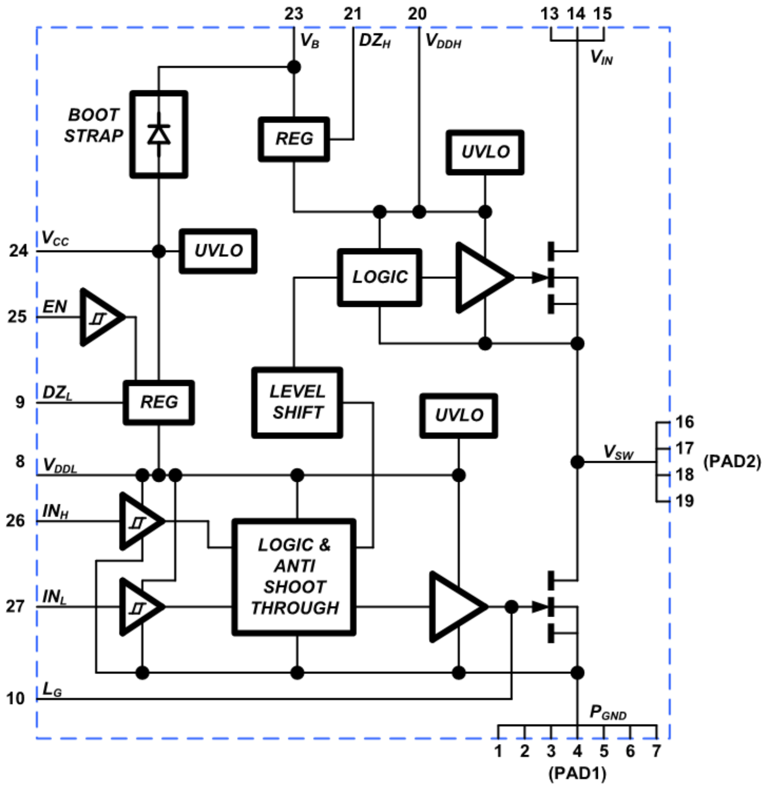
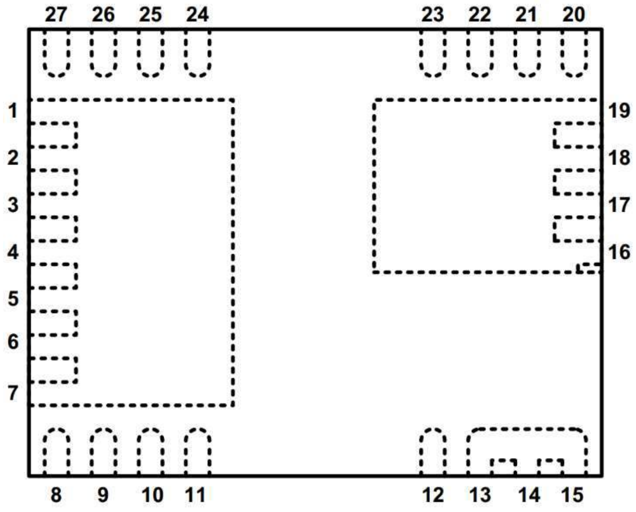


Fig 4: Propagation Delay Boost Mode t_{INLPHL}

Internal Schematic, Pin Configurations and Functions





(Top View)

Pin		I/O(1)	Description
Number	Symbol		
1 – 7 (and large pad)	P_{GND}	G	Power ground
8	V_{DDL}	P	Low-side drive supply
9	D_{ZL}	I	V_{DDL} set voltage (6.2V Zener to P_{GND})
10	L_G	O	Low-side gate
11	N/C		No connect
12	N/C		No connect
13 – 15	V_{IN}	P	HV input
16 – 19 (and small pad)	V_{SW}	O	Half-bridge switch Node
20	V_{DDH}	P	High-side drive supply
21	D_{ZH}	I	V_{DDH} set voltage (6.2V Zener to V_{SW})
22	N/C		No connect
23	V_B	P	High-side gate driver bootstrap rail
24	V_{CC}	P	IC supply voltage
25	EN	I	IC enable input (1=ON)
26	IN_H	I	High-side drive input
27	IN_L	I	Low-side drive input

(1) I = Input, O = Output, P = Power, G= Ground, M = Monitor

Functional Description

This GaN Power IC includes many functions designed for proper half-bridge operation during different circuit operating modes. The following functional description contains additional information regarding the IC operating modes and pin functionality.

Start-Up

Integrated into the design are UVLO circuits for disabling the IC when V_{CC}, V_{DDL} and V_B are below their respective UVLO+ thresholds. During UVLO Mode, the gate drive and half-bridge power FETs are disabled and V_{CC} consumes a low current. At start-up when the V_{CC} supply voltage increases (Fig 5), the voltages at the V_{DDL} pin and the DZ_L pin both increase as well. The V_{DDL} supply voltage will exceed the V_{DDUV+} threshold (4.8V typical) and then get limited by the internal regulator to the voltage level set by the Zener diode at the DZ_L pin (6.2 V, typical). The Zener diodes at the DZ_L and DZ_H pins should be a low-current type with a flat Zener voltage curve (above the knee) in the sub-100 µA current range (see Table I for recommended Zener diode part numbers). The V_{CC} voltage continues to increase until it exceeds the VCC_{UV+} threshold (9.25V typical) and the IC enters Normal Operating Mode. Initially, only the low-side half-bridge FET will turn on with the IN_L PWM input signal. The high-side supply V_B charges up through the internal bootstrap FET during the IN_L on-time. When V_B exceeds the VB_{UV+} threshold (9.25V typical), the high-side circuitry will be enabled and the high-side FET will turn on with the next IN_H PWM input signal.

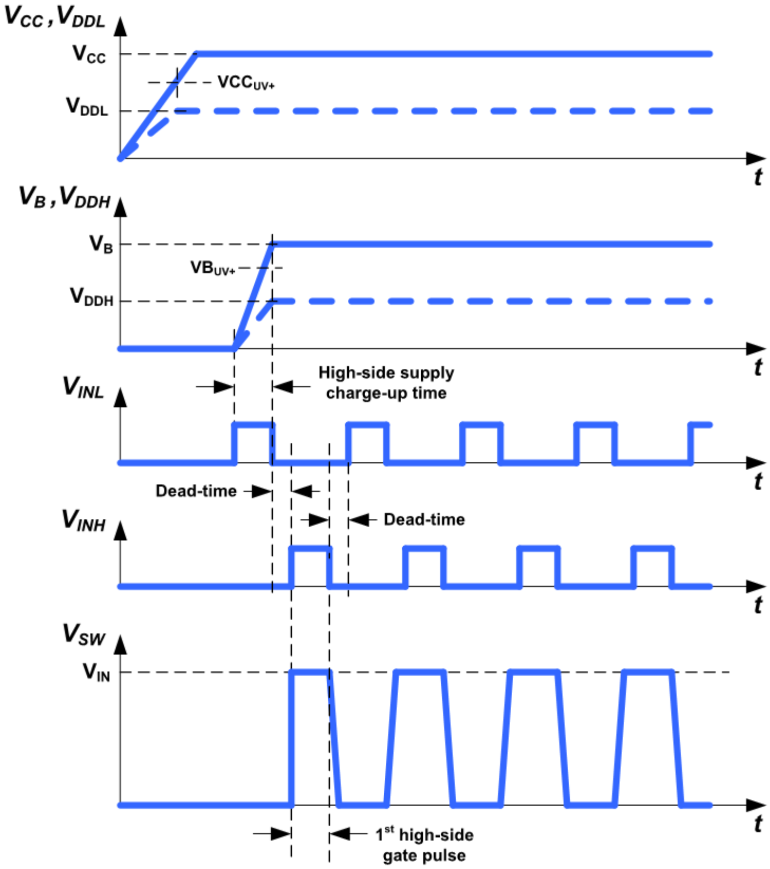


Fig. 5. Start-up timing diagram

Functional Description (cont.)

Normal Operating Mode

During normal operating mode, the EN pin is above the V_{EN+} threshold (4V maximum), V_{CC} is being regulated at a sufficient level (15 V typical) by the auxiliary power supply of the power converter, and V_B is at a sufficient level (as set by V_{CC} and the internal bootstrap circuit). The PWM input signals at the IN_L and IN_H pins turn the gates of the internal high- and low-side power FETs on and off at the desired duty-cycle, frequency and dead-time. The input logic signal at the IN_L pin turns the low-side half-bridge power FET on and off (0=OFF, 1=ON), and the input logic signal at the IN_H pin turns the high-side half-bridge power FET on and off (0=OFF, 1=ON). As the PWM inputs are turned on and off in a complementary manner each switching cycle, the V_{SW} pin (half-bridge mid-point) is then switched between P_{GND} (IN_L=1, IN_H=0) and V_{IN} (IN_L=0, IN_H=1) at the given frequency and duty-cycle (Fig. 6). This Power GaN IC includes shoot-through protection circuitry that prevents both power FETs from turning on simultaneously. The IC also includes an internal bootstrap FET for supplying the high-side circuitry. The bootstrap FET is enabled during normal operating mode and is turned on each PWM switching cycle only when the IN_L pin is ‘HIGH” and the low-side power FET is on. This will allow the V_B capacitor to be charged up each switching cycle for properly maintaining the necessary high-side supply voltage. The V_B capacitor value should be sized correctly such that the V_B voltage is maintained at a sufficient level above UVLO- during normal operation. Should the V_B-V_{SW} voltage decrease below the falling VB_{UV-} UVLO threshold (8.75V typical) at any time, then the high-side power FET will turn off and become disabled until V_B-V_{SW} increases again above the VB_{UV+} threshold (9.25V typical).

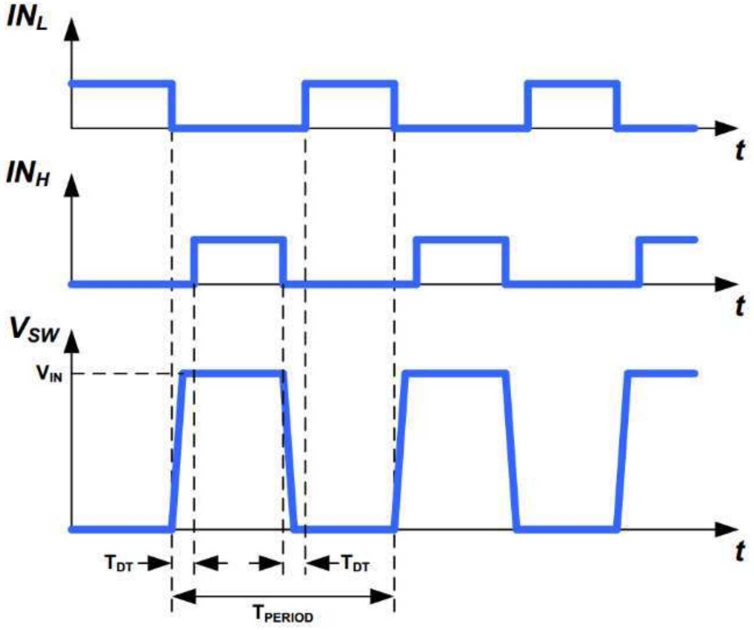


Fig. 6. PWM inputs and V_{SW} output voltage timing diagram during normal ZVS operation

Functional Description (cont.)

Programmable Turn-on dV/dt Control

During first start-up pulses or during hard-switching conditions, it is desirable to limit the slew rate (dV/dt) of the drain of the low-side power FET during turn-on. This is necessary to reduce EMI or to reduce circuit switching noise. The turn-on slew rate of the low-side power FET is already reduced by default internally to a low level. To reduce the turn-on dv/dt rate of the internal low-side power FET further, an external capacitor (C_{LG}) can be placed at the L_G pin. This capacitor value should be 300pF typical and 600pF max (see Table I). The slew rate will decrease with increasing C_{LG} (Figure 7). If further reduction of the slew rate is needed, a resistor (R_{DD}) can be placed in between the V_{DD} capacitor and the V_{DD} pin. This resistor value should be 0 Ω typical and 20 Ω max (see Table I).

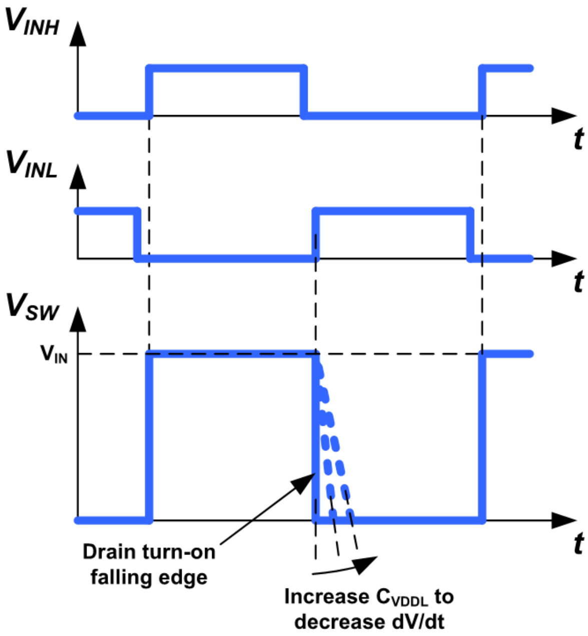


Fig. 7. Low-side turn-on dv/dt slew rate control

SYM	DESCRIPTION	MIN	TYP	MAX	UNITS
C_{LG}	C_{LG} gate capacitor		300	600	pF
R_{VDDL}	R_{VDDL} resistor		0	20	Ω

Table I. Low-side FET slew rate control recommended component values.

Functional Description (cont.)

Standby Mode

This GaN Power IC includes an Enable input (EN pin) for disabling the IC and reducing the V_{CC} current consumption. To disable the IC and enter low-current Standby Mode, the EN pin is decreased below the V_{EN-} threshold (1V min). This will disable both half-bridge FETs and reduce V_{CC} current consumption to a low level 130 uA typical). DZ_L will remain held at its Zener voltage and V_{DDL} will slowly discharge to P_{GND}. When the EN pin voltage is increased again above the V_{EN+} threshold (4V max), the IC will become enabled and V_{DDL} will charge up again above the V_{DDUV+} threshold and the IC will start up (Fig. 8). An external MOSFET can be used to pull the EN pin down to the P_{GND} potential. If an enable signal is available that is greater than the V_{DDL} voltage, then a diode can be used to pull down the EN pin. If an active standby signal is available from the controller then this signal can be used to pull down the EN pin directly with no additional external components required.

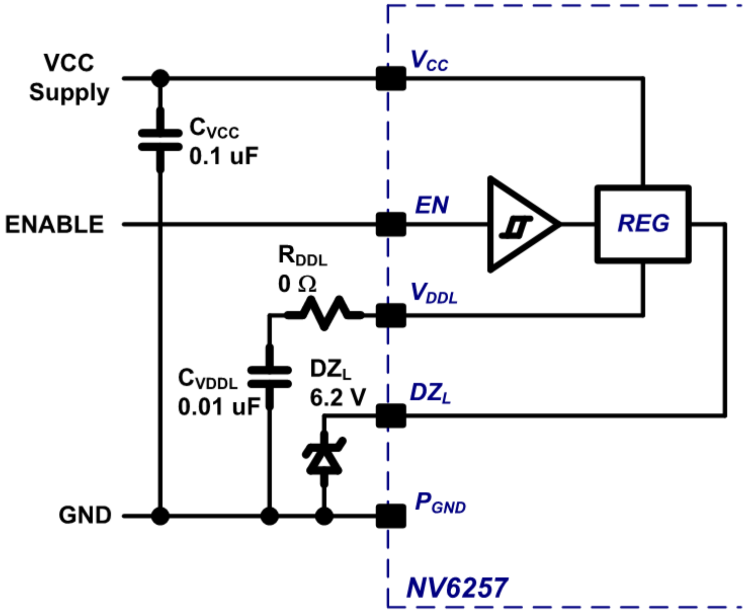


Fig. 8. Enable input connection diagram.

Functional Description (cont.)

Connection Diagram

The following schematic (Figure 9) and table (Table II) shows the typical connection diagram and recommended component values for the external filter capacitors and Zener diodes connected to the pins of this GaN Power IC. These components should be placed as close as possible to the IC. Please see PCB Layout Guidelines for more information.

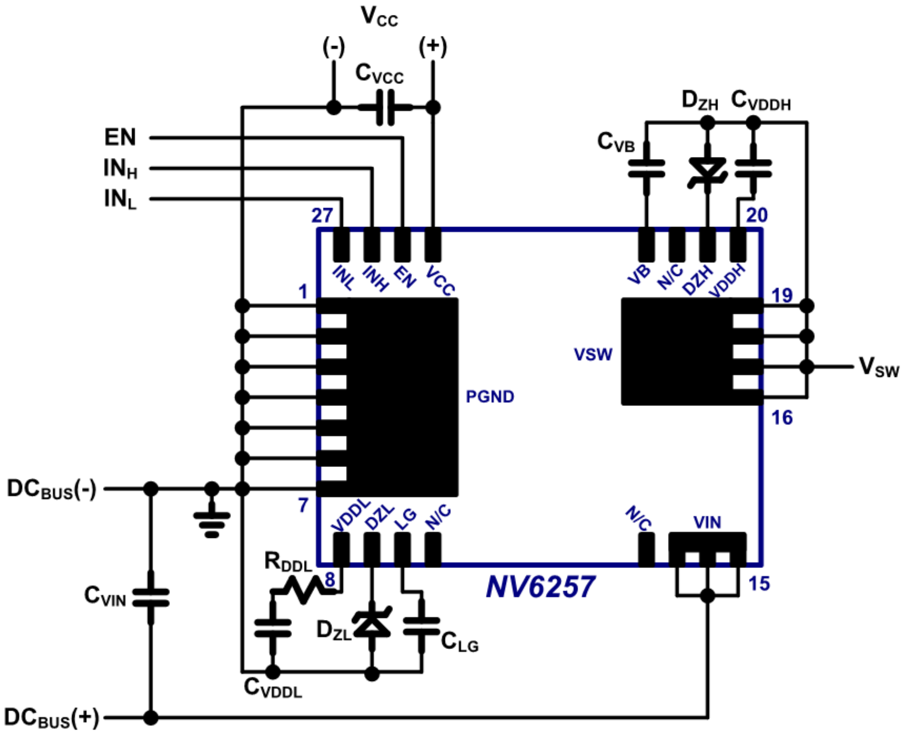


Fig. 9. Typical connection diagram.

Functional Description (cont.)

Component Values

The following table (Table II) shows the recommended component values (typical only) for the external filter capacitors and Zener diode connected to the pins of the NV6257. These components should be placed as close as possible to the IC. Please see PCB Layout guidelines for more information. The Zener diode at the DZL,H pins should be a low-current type with a flat Zener knee.

SYM	DESCRIPTION	TYP	UNITS
C_{VCC}	V_{CC} supply filter capacitor	0.1	µF
$C_{VDDL,H}$	V_{DDL} and V_{DDH} supply capacitors	0.01	µF
C_{VB}	V_B supply capacitor	0.1	µF
C_{LG}	C_{LG} gate capacitor	300	pF
R_{VDDL}	R_{VDDL} resistor	0	Ω

Table II. Recommended component values (typical only).

Zener Diode Selection

The Zener voltage is a critical parameter that sets the internal reference for gate drive voltage and other circuitry. The Zener diode needs to be selected such that the voltage on the $DZ_{L,H}$ pins are within their recommended operating conditions (5.8 V to 6.6 V) across operating temperature (-40° C to 125° C) and bias current (10 µA to 1 mA). To ensure effective operation, the current vs. voltage characteristics of the Zener diode should be measured down to 10µA to ensure flat characteristics across the current operating range (10 µA to 1 mA). The recommended part numbers meet these requirements (see Table II). If the Zener selected by user does not ensure that the voltage on the $DZ_{L,H}$ pins are always within their recommended operating range, the functionality and reliability of the IC can be impacted.

Only the following Zener diodes are to be used with this GaN Power IC (Table III):

SYM	DESCRIPTION	PART NO.	SUPPLIER	TYP	UNITS
$DZ_{L,H}$	V_{DDL} and V_{DDH} set Zener diode (DZ_L and DZ_H pins)	BZT52B6V2 RHG	Taiwan Semiconductor Corporation	6.2	V
		MM3Z6V2ST1G	ON-Semiconductor		
		PDZ6.2B.115	Nexperia (NXP)		
		PLVA662A.215	Nexperia (NXP)		
		LM3Z6V2T1	Leshan Radio Company		

Table III. Qualified Zener diode components to be used with this GaN Power IC.

Functional Description (cont.)

PCB Layout Guidelines

The design of the PCB layout is critical for good noise immunity, sufficient thermal management, and proper operation of the IC. A typical PCB layout example is shown on page 16. The following rules should be followed carefully during the design of the PCB layout:

1) Place all IC filter and programming components directly next to the IC. These components include (C_{VCC}, C_{VDDL}, R_{DDL}, DZ_L, C_{LG}, C_{VB}, C_{VDDH}, DZ_H).

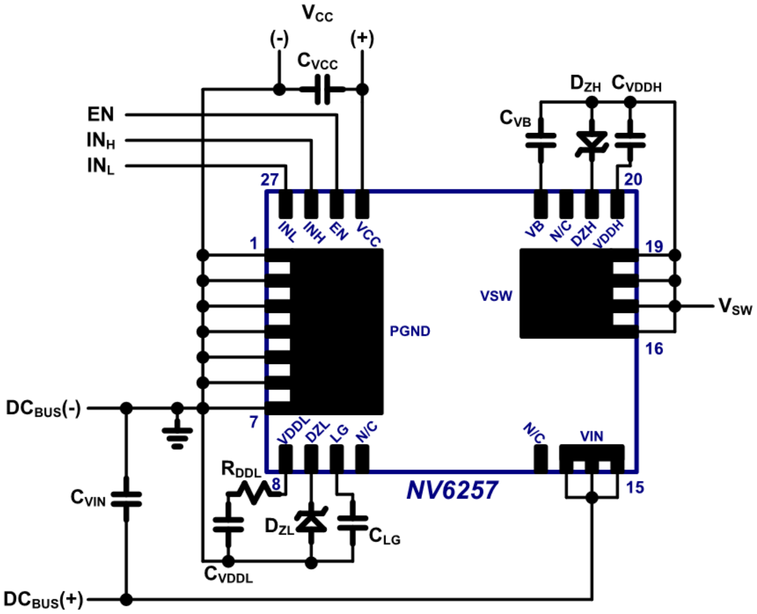
2) Keep the ground trace of IC filter and programming components separate from P_{GND} trace. The ground trace of the IC filter and programming components should connect to the P_{GND} at a single point only. Do not run high P_{GND} currents through the low current ground trace of the filter components!

3) For best thermal management, place thermal vias in the P_{GND} and V_{SW} pad areas to conduct the heat out through the bottom of the package and through the PCB board to other layers.

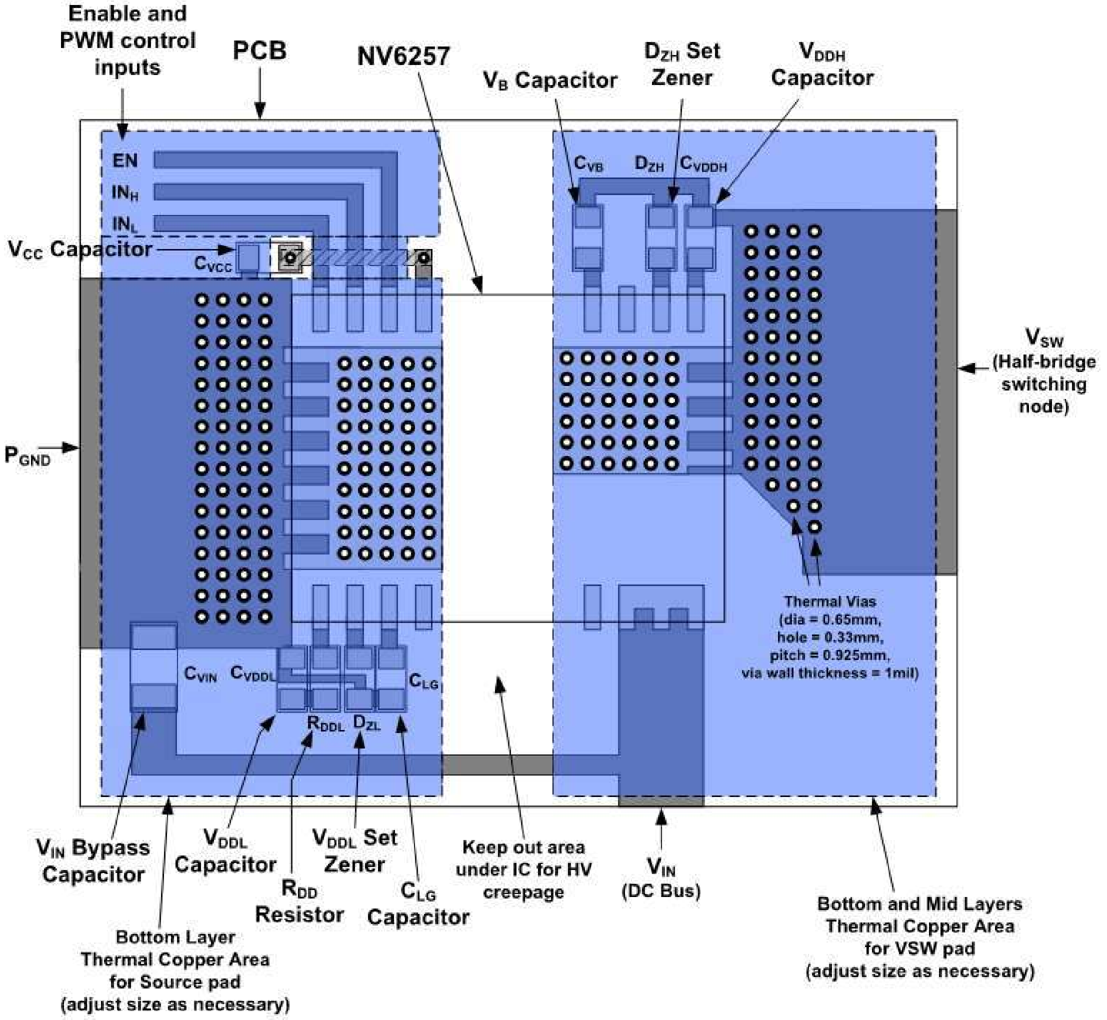
4) Use large PCB thermal planes (connected with thermal vias to the P_{GND} and V_{SW} pads) and additional PCB layers to reduce IC temperatures as much as possible.

5) For multi-layer boards, do not place V_{SW} copper areas across P_{GND}-referenced components, and, do not place P_{GND} copper areas across V_{SW}-referenced copper areas. Keep them separate to avoid capacitive noise coupling between the low-side and high-side circuitry and to avoid possible faulty switching.

PCB Layout Guidelines (2-layer board)

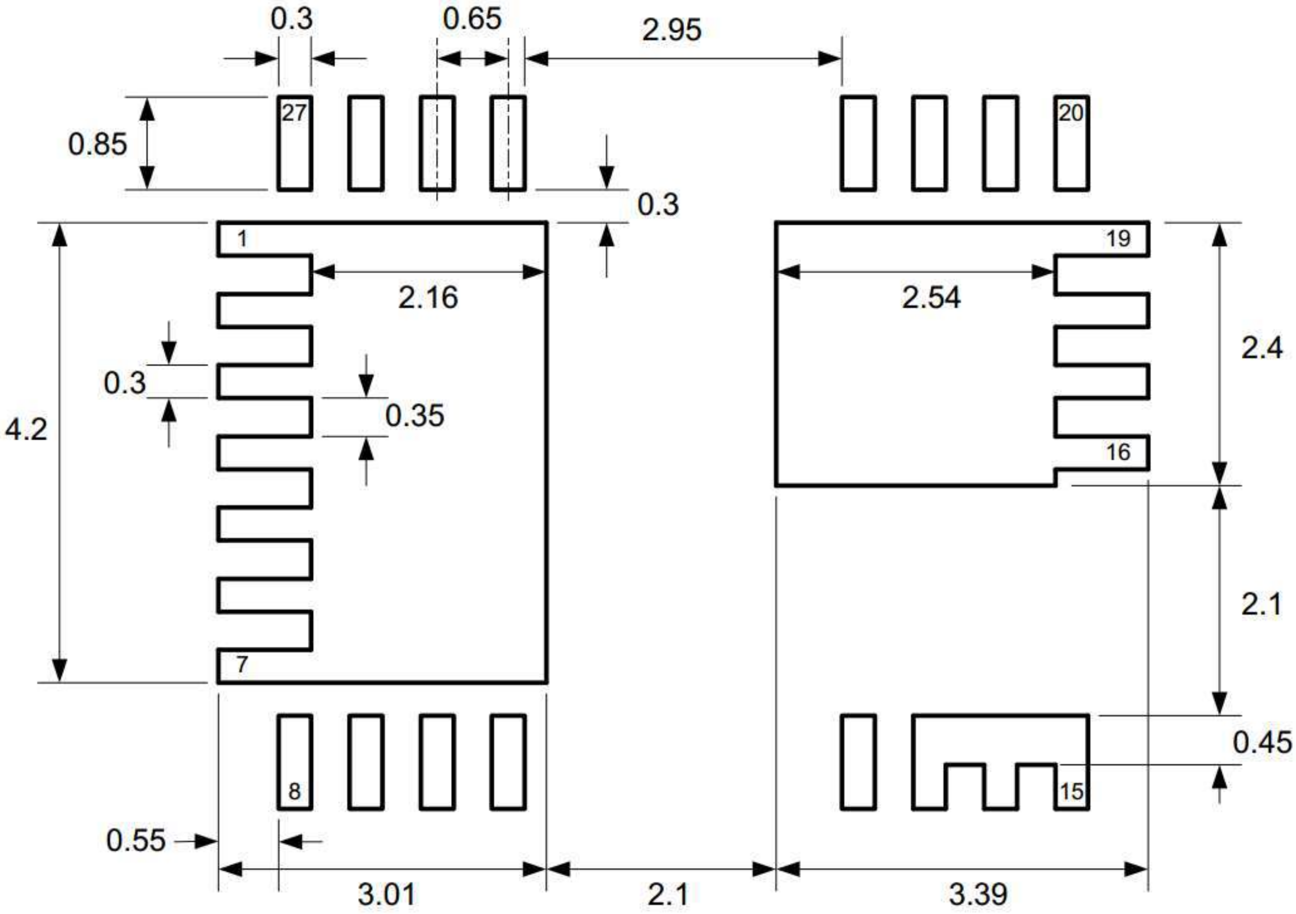


○ Via
▭ PCB
▬ Top Layer
▭ Bottom and Mid Layers
▭ Component Landing Pad (Top Layer)



(Top View)

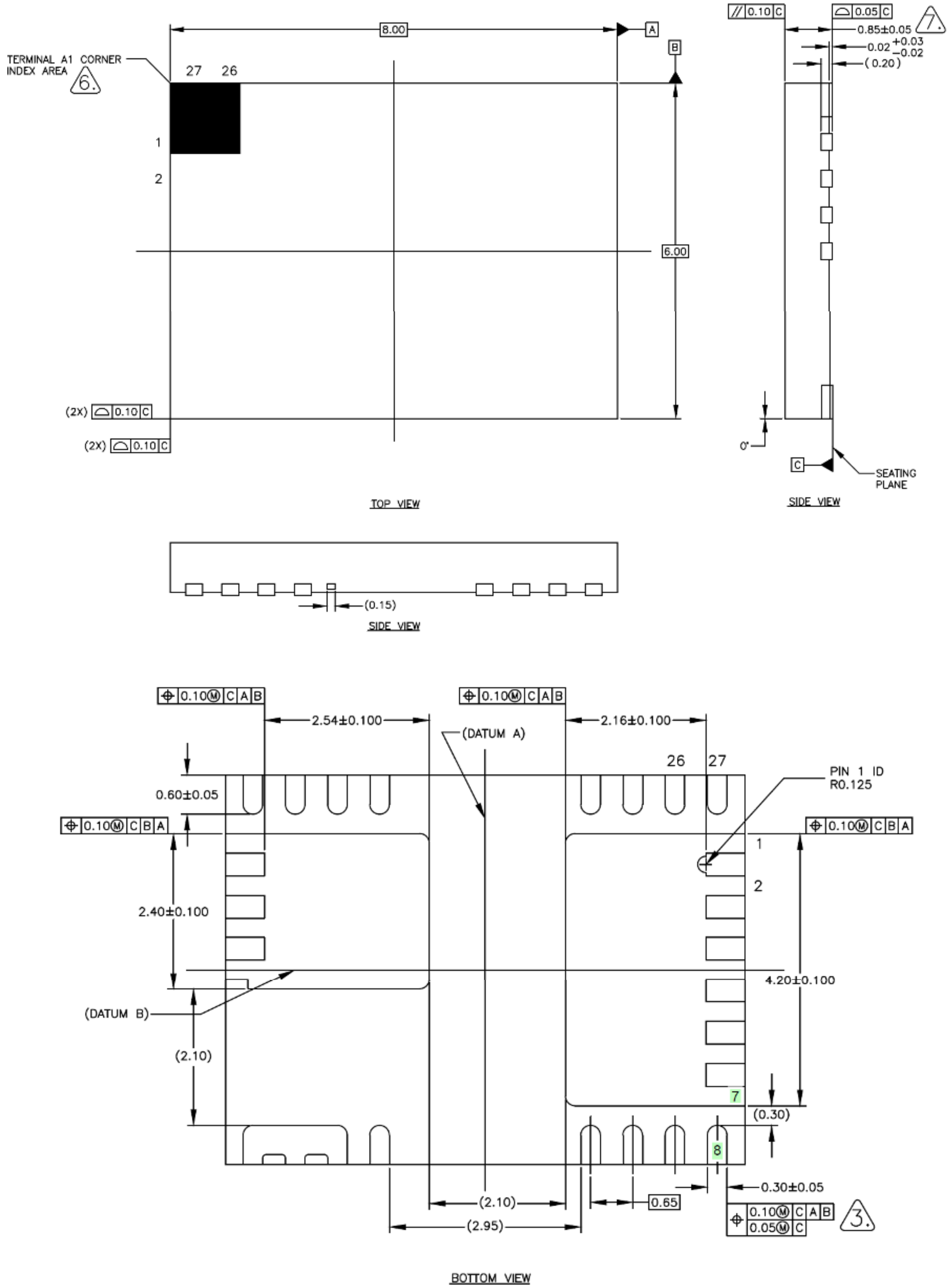
Recommended PCB Land Pattern



(Top View)

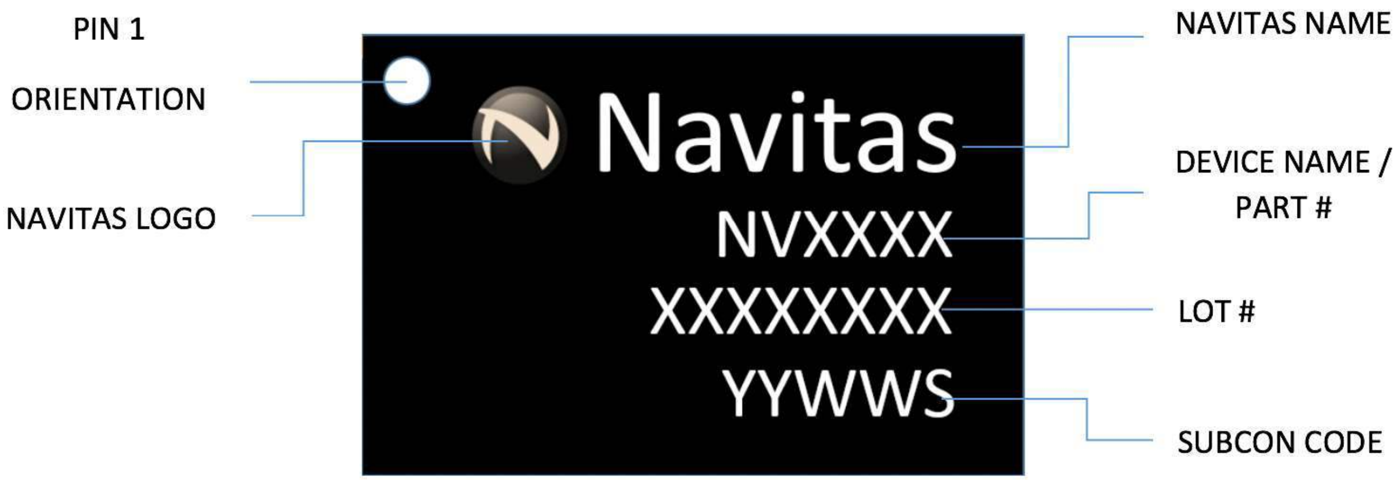
All dimensions are in mm

Package Outline (Power QFN)



All dimensions are in mm

Part Marking Information



Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Package	MSL Rating	Packing
NV6257	-55°C to +150°C T_{CASE}	-55°C to +150°C T_{CASE}	6 x 8 mm PQFN	3	Tape & Reel

Revision History

Date	Status	Notes
8-1-18	TARGET	First publication

Additional Information

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