
Switchtec™ Low Lane Count PCIe® Gen4x16 Switch Family with Multi-Host Support

Features

- **High-Performance Non-Blocking Switch**

- PCIe Gen4x16 switch
- Up to 256 GB/s switching capacity
- Full line rate on all ports, 16GT/s per lane
- Ports bifurcate to x2/x4 lanes, x1 devices can be enumerated on any port
- Non-Transparent Bridge (NTB) supported for Root Complex (RC) connections
- NT address translation using direct windows and multiple sub-windows per BAR
- Configurable domains for RC ports

- **Power Management**

- Active State Power Management (ASPM)
- Software controlled power management
- Supports L0, L1, L2, L3 link states

- **PCIe Interfaces**

- Passive, managed, and optical cable support

- **Peripheral I/O Interfaces**

- SPI interface for external boot memory
- FlexCom I/O block configurable for USART, SPI, I²C & TWI
- Secure JTAG and EJTAG interface
- GPIO pins

- **Reliability and Availability**

- Advanced error reporting (AER) on all ports

- **Firmware Security**

- OEM-controlled Root of Trust for firmware and configuration signing
- Secure Boot from SPI flash
- Secure firmware updates
- Secure RMA - OEM-controlled Root of Trust for Secure JTAG interface

- **ChipLink Diagnostic Tools**

- Extensive debug, diagnostics, configuration and analysis tools with an intuitive GUI
- Access to configuration data, management capabilities, and signal integrity analysis tools (such as real-time eye capture)
- Errors, statistics, performance, and TLP latency counters
- Connects to device over in-band PCIe or sideband signals (UART and TWI)

- **Package**

- 353-ball FCCSP (16 x 16 mm) package

- **Environmental**

- Commercial temperature (0°C to +70°C)
- Industrial temperature (-40°C to +85°C)
- Automotive AEC-Q100 Qualified Grade 2 temperature (-40°C to +105°C)
(PCI1003/PCI1004 *only*)

Target Applications

- Level 2/3 Advanced Driver-Assistance Systems (ADAS)
- Defense & Aerospace Compute Applications
- Embedded Servers & Industrial PCs
- Video Acceleration Equipment

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1.0 INTRODUCTION

1.1 General Description

The low-lane count PCI100x family builds on the legacy of the high-performance Microchip Switchtec family. The PCI100x family of products offers many features of the full-size data center switches in a small lane count format, enabling PCIe connectivity and flexible system design. The smaller form factor makes the products suitable for SoC and accelerator connectivity as well as fanout of port- and lane-limited PCIe connections. The PCI Gen4 switch family is composed of a PCIe Base Specification 4.0 compliant switch supporting up to 16 lanes with Non-Transparent Bridge (NTB) options, embedded lower power states, and diagnostics and debug capabilities.

Preconfigured product variants offer options with up to 8 ports. All ports are NTB-capable, with some ports preconfigured, depending on the selected product family variant. Depending on the product selected, port lane counts are available in x2 and x4 widths. All ports can be used with reduced lane counts when required by the connecting a Root Complex (RC) or End Point (EP). Independent software domains enable direct access from RC devices to domain ports. Non-Transparent Bridging enables access to resources in other domains. “Cut-through” mode is supported for switching packets and advanced power saving features include idling of empty ports and clock removal during L1 states.

End-to-end data integrity protection and low latency performance is consistent with other Switchtec products. Typical packet latency is 120ns for port-to-port transit.

Comprehensive diagnostics and debugging are available through the ChipLink tool suite. Diagnostic capabilities include PCIe Analyzer and configurable Stack Error Counters, Eye Opening Margining, and firmware logging. Secure boot and software updates are supported.

Typical applications for the PCI100x family of products include Automotive Level 2+ and Level 3 ADAS systems, defense and aerospace compute applications, embedded servers & industrial PCs, and small video systems.

To support safety applications, the PCI100x device family is fully ISO-26262 Functional Safety compliant and carries an ASIL-B rating. Extensive PCIe reporting capabilities combine with safety monitoring features to report status of switch functionality, data movement, and node connections.

The PCI100x family of products are available in commercial (0°C to +70°C), industrial (-40°C to +85°C), and AEC Q-100 Automotive grade 2 (-40°C to +105°C) temperature range versions.

[Table 1-1](#) provides a summary of the preconfigured variances between family members, including number of ports, Upstream Facing Port (UFP) configuration, Downstream Facing Port (DFP) configuration, number of NTBs, overall number of lanes, and temperature range options.

TABLE 1-1: PCI100X FAMILY FEATURE MATRIX

Part Number	Ports	UFP Config.	DFP Config.	NTBs	Lanes	Com. Temp	Ind. Temp	Auto. Temp
PCI1001 4-Port 0-NTB PCIe Gen4x16 Fanout Switch	4	1x4 Lane Port	3x4 Lane Ports	0	16	Yes	Yes	No
PCI1003 6-Port 4-NTB PCIe Gen4x16 Switch	6	2x4 Lane Ports & 2x2 Lane Ports	2x2 Lane Ports	4	16	Yes	Yes	Yes
PCI1004 4-Port 4-NTB PCIe Gen4x16 Switch	4	4x4 Lane Ports	0	4	16	Yes	Yes	Yes
PCI1005 7-Port 0-NTB PCIe Gen4x16 Fanout Switch	7	1x4 Lane Port	6x2 Lane Ports	0	16	Yes	Yes	No

PCI100X

An Internal block diagram and typical application block diagram for each of the devices in the PCI100x family are detailed in the following sub-sections.

1.1.1 PCI1001

FIGURE 1-1: PCI1001 INTERNAL BLOCK DIAGRAM

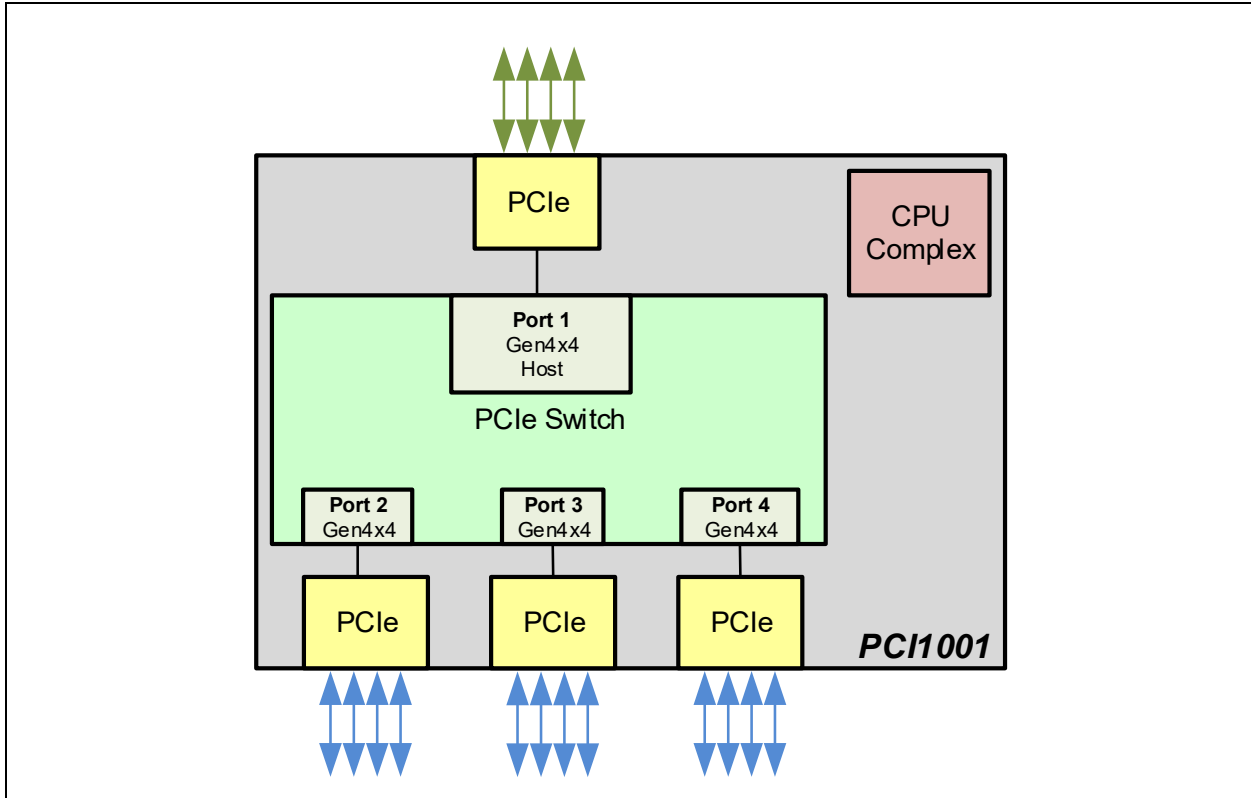


FIGURE 1-2: PCI1001 APPLICATION BLOCK DIAGRAM

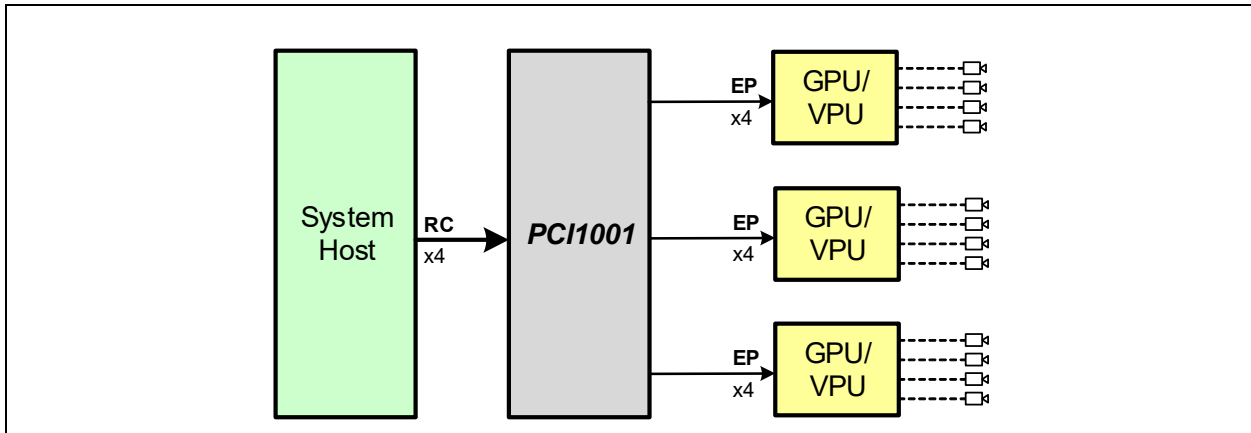


FIGURE 1-3: PCI1003 INTERNAL BLOCK DIAGRAM

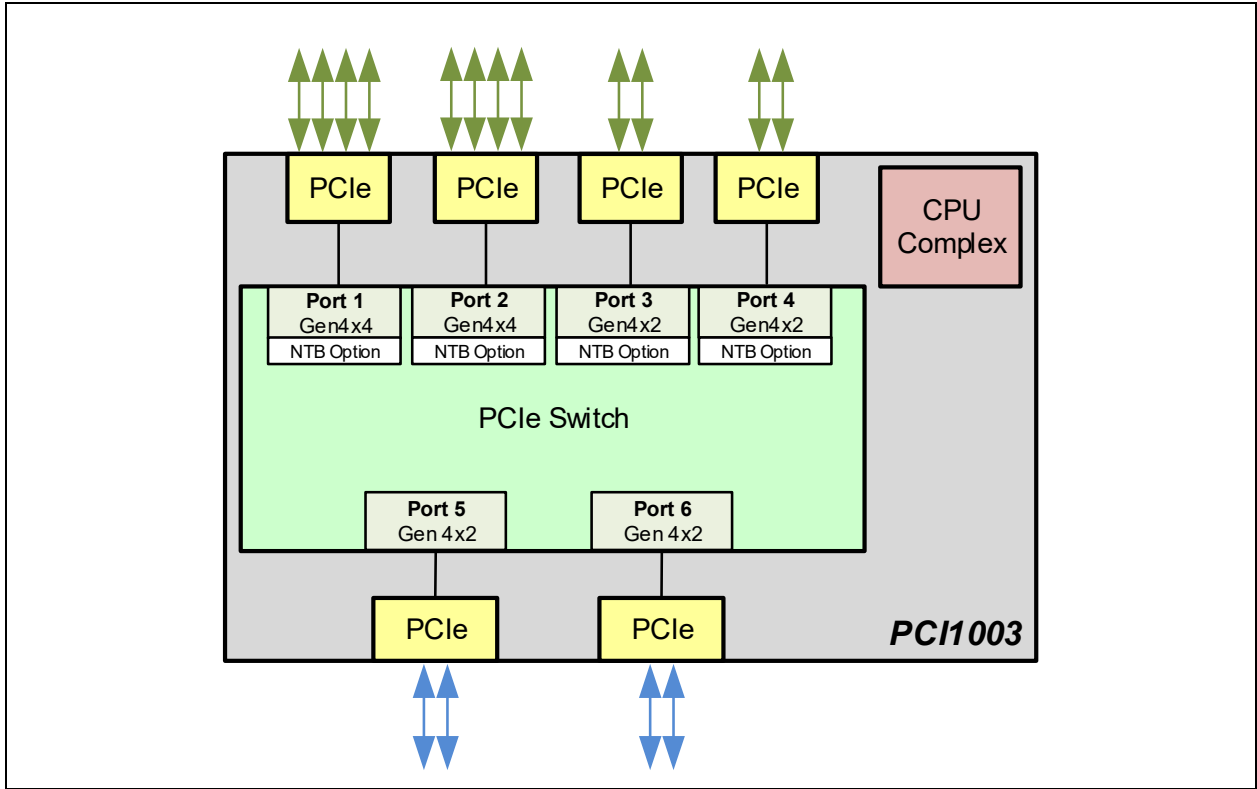
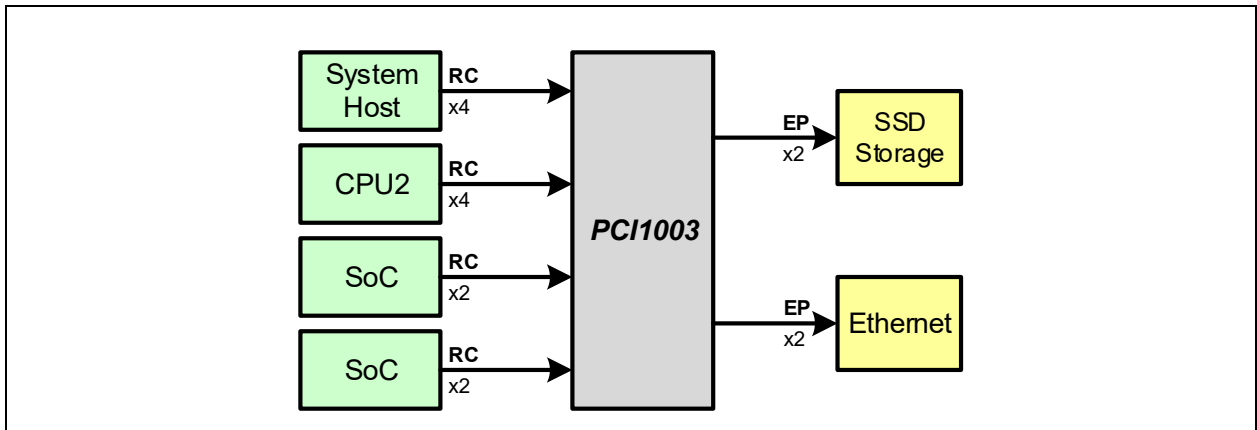


FIGURE 1-4: PCI1003 APPLICATION BLOCK DIAGRAM



PCI100X

1.1.3 PCI1004

FIGURE 1-5: PCI1004 INTERNAL BLOCK DIAGRAM

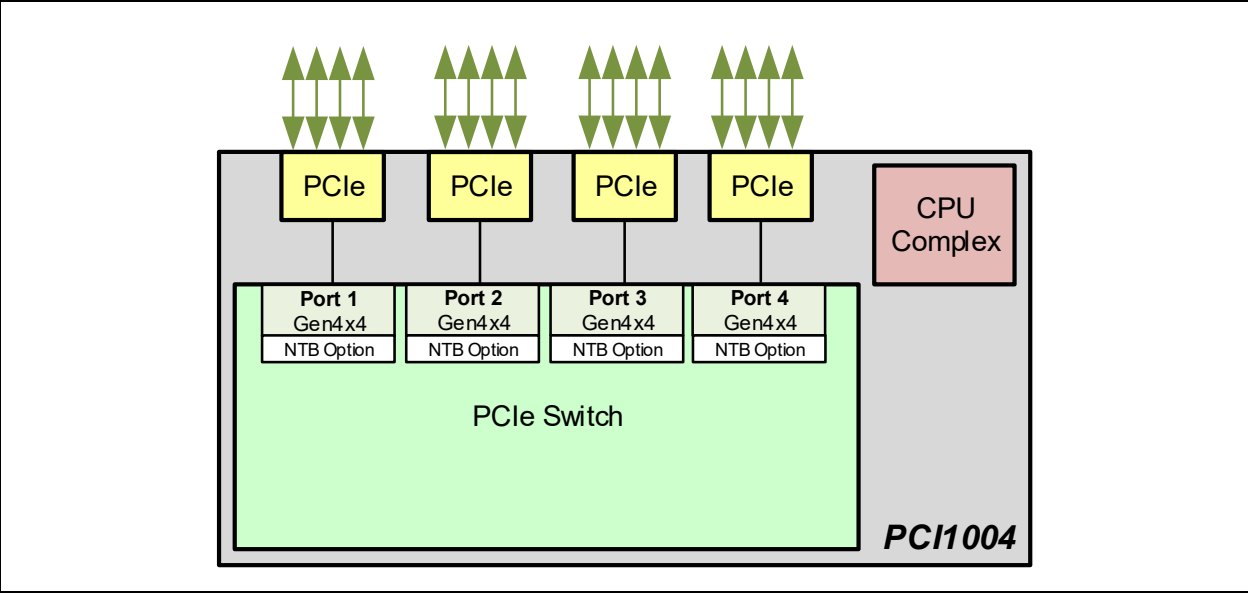


FIGURE 1-6: PCI1004 APPLICATION BLOCK DIAGRAM

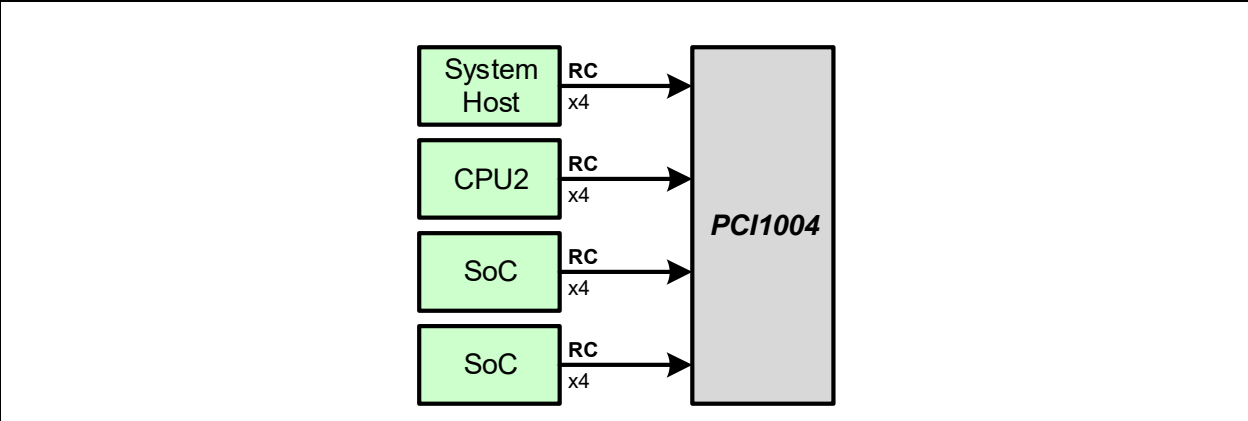


FIGURE 1-7: PCI1005 INTERNAL BLOCK DIAGRAM

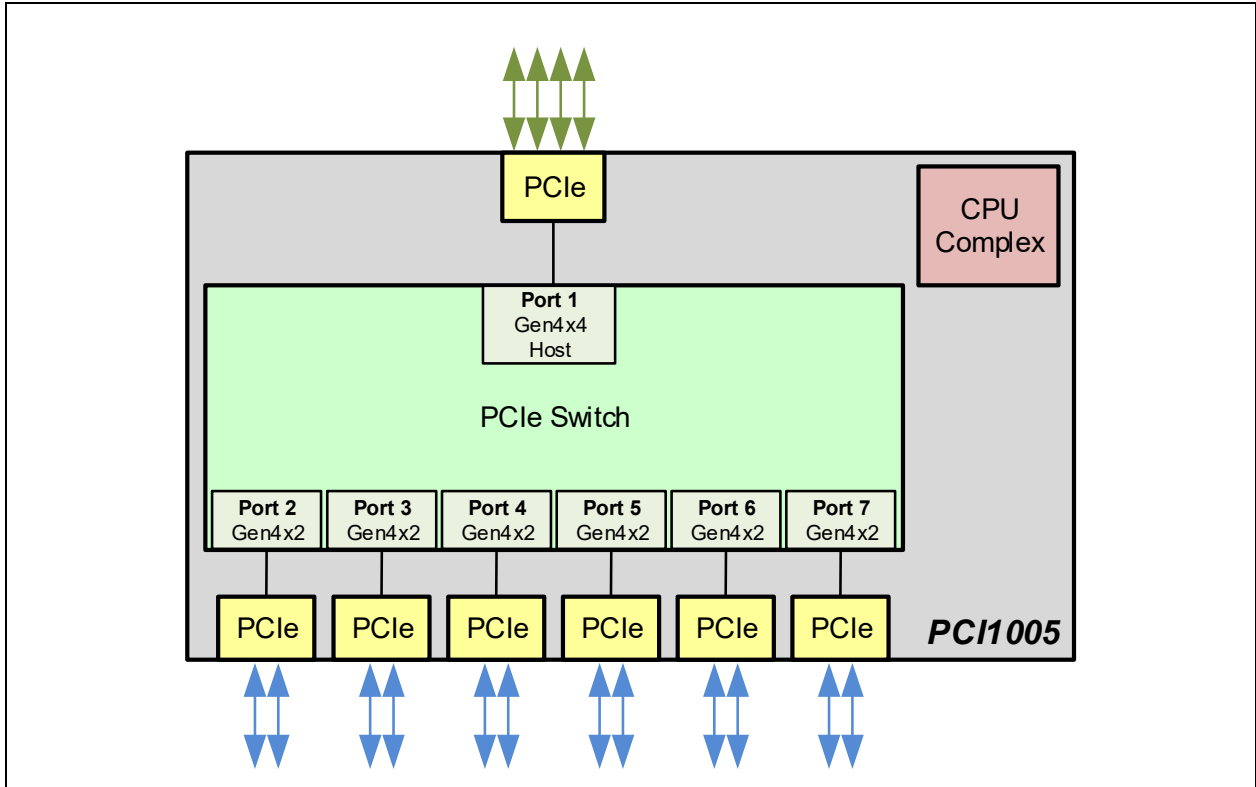
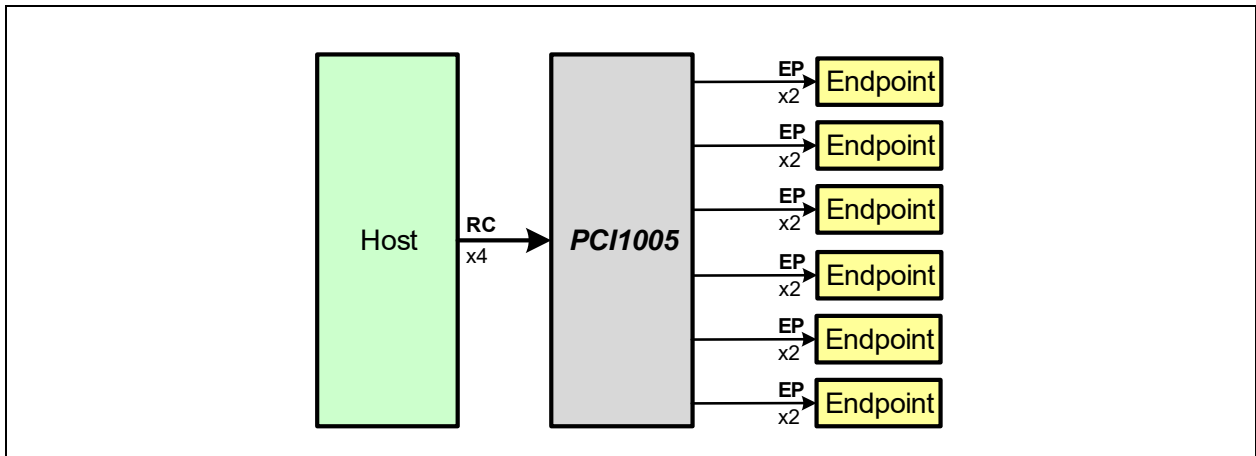


FIGURE 1-8: PCI1005 APPLICATION BLOCK DIAGRAM



PCI100X

2.0 PACKAGE INFORMATION

Note: For the most current package drawings, see the Microchip Packaging Specification at: <http://www.microchip.com/packaging>.

2.1 Package Drawing & Dimensions

FIGURE 2-1: 353-FCCSP PACKAGE (DRAWING)

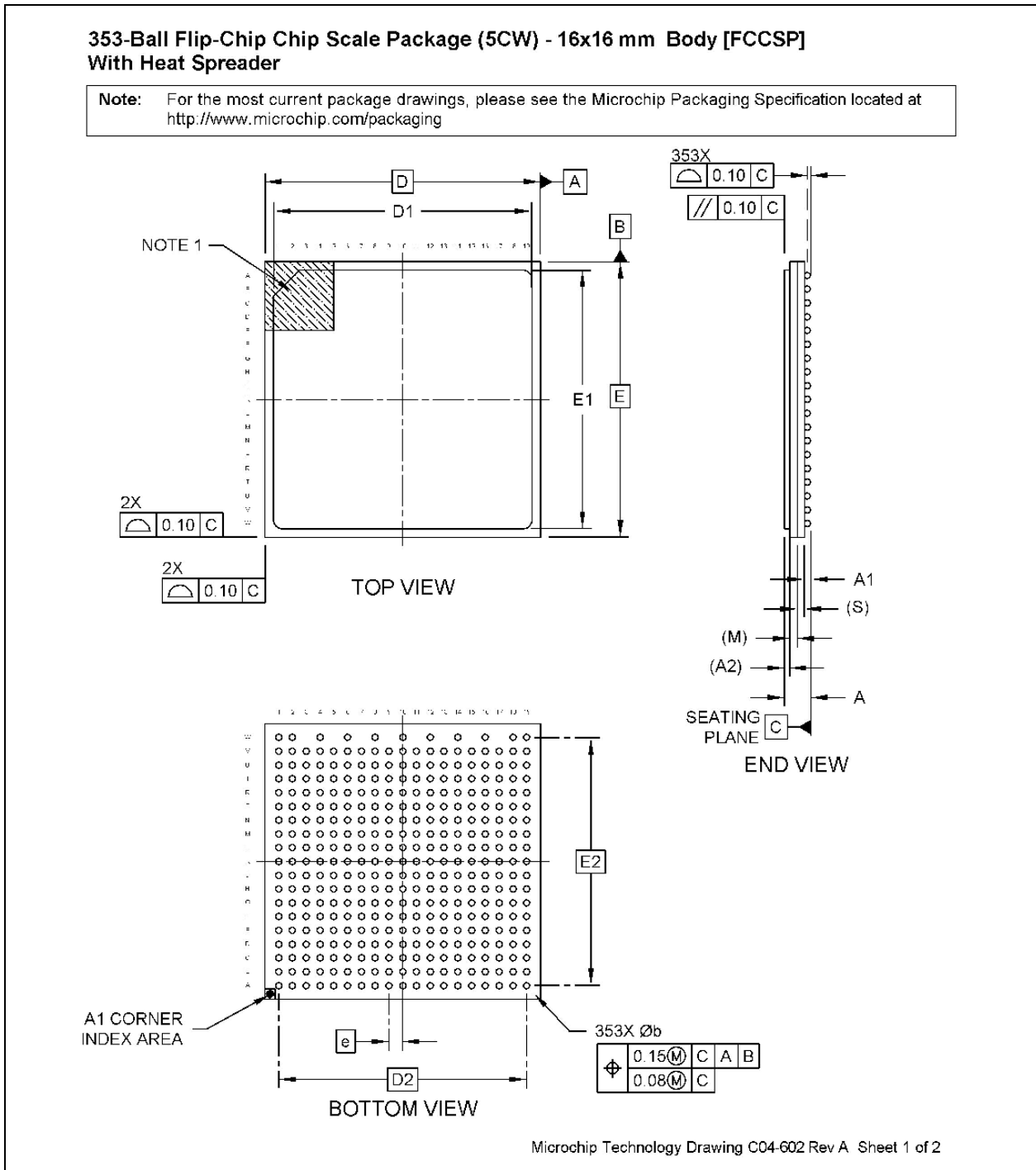
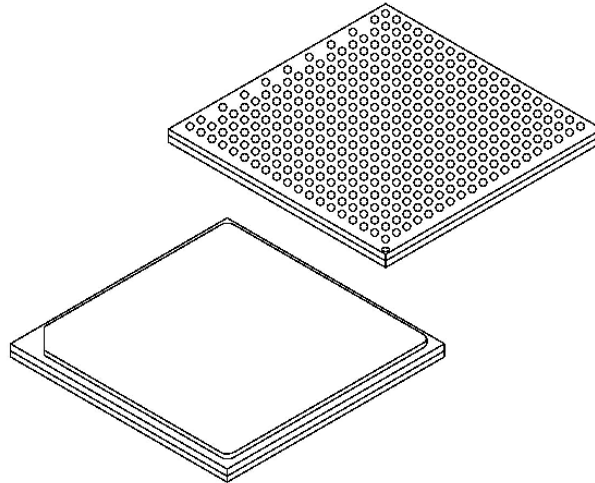


FIGURE 2-2: 353-FCCSP PACKAGE (DIMENSIONS)

**353-Ball Flip-Chip Chip Scale Package (5CW) - 16x16 mm Body [FCCSP]
With Heat Spreader**

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



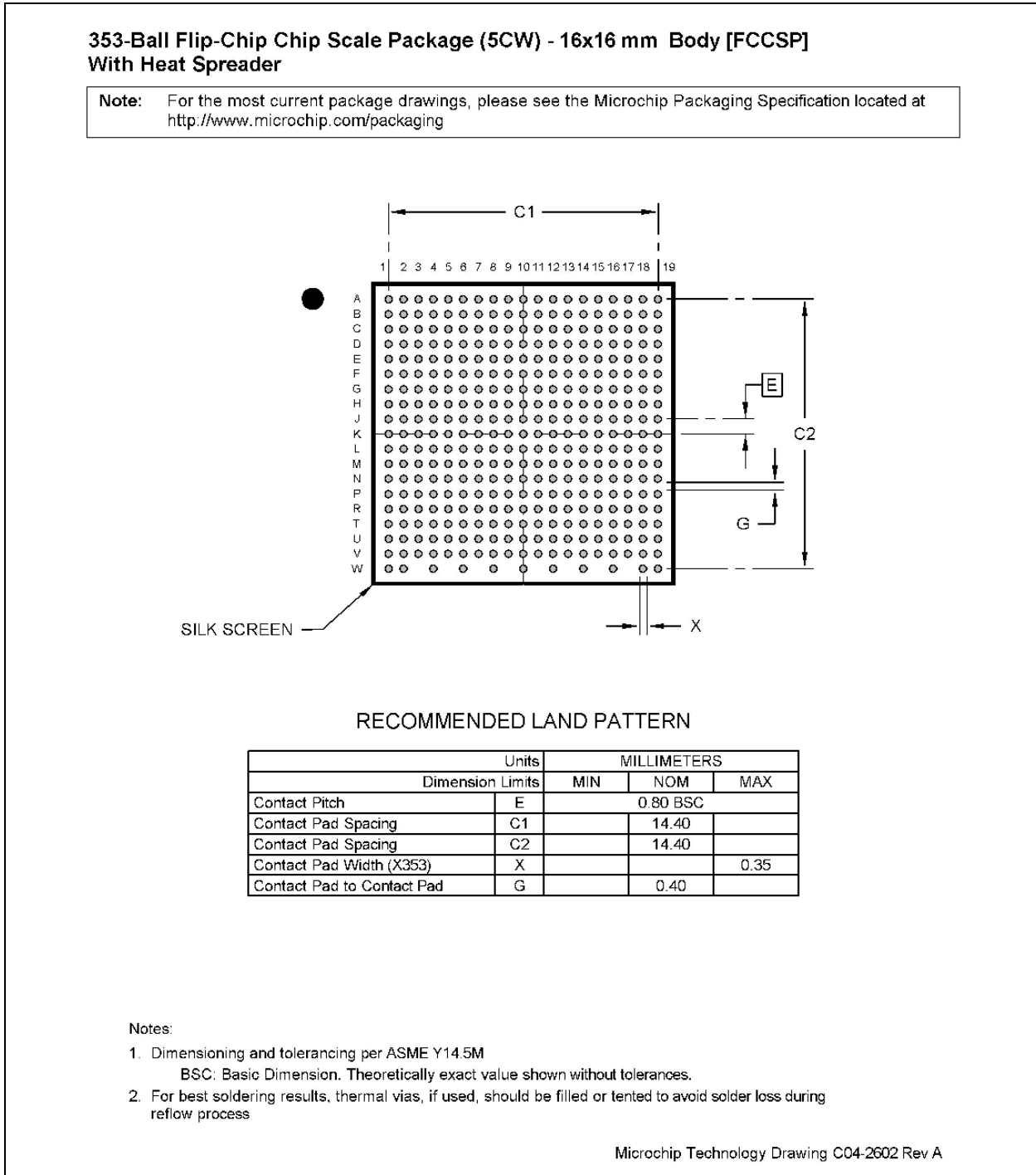
Dimension	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	353 BSC		
Pitch	e	0.80 BSC		
Overall Height	A	1.34	1.44	1.54
Ball Height	A1	0.27	0.32	0.37
Heat Sink Thickness	A2	0.20 REF		
Mold Thickness	M	0.45 REF		
Substrate Thickness	S	0.41 REF		
Overall Length	D	16.00 BSC		
Heat Sink Length	D1	14.95	15.00	15.05
Ball Array Length	D2	14.40 BSC		
Overall Width	E	16.00 BSC		
Heat Sink Width	E1	14.95	15.00	15.05
Ball Array Width	E2	14.40 BSC		
Ball Diameter	b	0.36	0.41	0.46

Notes:

- Pin 1 visual index feature may vary but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

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FIGURE 2-3: 353-FCCSP PACKAGE (LAND-PATTERN)



APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005055C (01-14-25)	All	<p>First public document release.</p> <p>Updated package and ordering information.</p> <p>Removed the following bullet under “High-Performance Non-Blocking Switch” shown on the cover: “Optional 4-lane cross-link port for up to 24-lanes and 6x NTB ports”</p> <p>Modified the following features on the cover:</p> <p>Power Management: Replaced “Supports L0, L1, L1.1, L1.2 power savings states” with “Supports L0, L1, L2, L3 link states”. Modified feature in ChipLink</p> <p>Diagnostic Tools: Replaced “Connects to device over in-band PCIe or sideband signals (UART, TWI and EJTAG)” with “Connects to device over in-band PCIe or sideband signals (UART and TWI)”.</p>
	All	Updated all package references from “FCBGA” to “FCCSP” throughout document.
	Section 2.1, Package Drawing & Dimensions	Updated package drawings
	Product Identification System	Updated to make consistent with datasheet layout/format.
DS00005055B (02-14-24)	All	Updated document to be in line with latest SKU matrix and package information
	Section 1.1, General Description	Added new paragraph
DS00005055A (08-07-23)	All	Initial Release

PCI100X

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	Tape & Reel / Tray	Temperature Range	Package	Part Number
PCI1001 4-Port: 1x4UFP 3x4DFP 0 NTBs	Tray	0°C to +70°C (Commercial)	353-ball FCCSP (16 x 16 mm)	PCI1001/5CW
	Tray	-40°C to +85°C (Industrial)	353-ball FCCSP (16 x 16 mm)	PCI1001-I/5CW
	Tape & Reel	0°C to +70°C (Commercial)	353-ball FCCSP (16 x 16 mm)	PCI1001T/5CW
	Tape & Reel	-40°C to +85°C (Industrial)	353-ball FCCSP (16 x 16 mm)	PCI1001T-I/5CW
PCI1003 6-Port: 2x4UFP 2x2UFP 2x2DFP 4 NTBs	Tray	0°C to +70°C (Commercial)	353-ball FCCSP (16 x 16 mm)	PCI1003/5CW
	Tray	-40°C to +85°C (Industrial)	353-ball FCCSP (16 x 16 mm)	PCI1003-I/5CW
	Tray	-40°C to +105°C (AEC-Q100 Auto)	353-ball FCCSP (16 x 16 mm)	PCI1003-V/5CWVAO
	Tape & Reel	0°C to +70°C (Commercial)	353-ball FCCSP (16 x 16 mm)	PCI1003T/5CW
	Tape & Reel	-40°C to +85°C (Industrial)	353-ball FCCSP (16 x 16 mm)	PCI1003T-I/5CW
	Tape & Reel	-40°C to +105°C (AEC-Q100 Auto)	353-ball FCCSP (16 x 16 mm)	PCI1003T-V/5CWVAO
PCI1004 4-Port: 4x4UFP 4 NTBs	Tray	0°C to +70°C (Commercial)	353-ball FCCSP (16 x 16 mm)	PCI1004/5CW
	Tray	-40°C to +85°C (Industrial)	353-ball FCCSP (16 x 16 mm)	PCI1004-I/5CW
	Tray	-40°C to +105°C (AEC-Q100 Auto)	353-ball FCCSP (16 x 16 mm)	PCI1004-V/5CWVAO
	Tape & Reel	0°C to +70°C (Commercial)	353-ball FCCSP (16 x 16 mm)	PCI1004T/5CW
	Tape & Reel	-40°C to +85°C (Industrial)	353-ball FCCSP (16 x 16 mm)	PCI1004T-I/5CW
	Tape & Reel	-40°C to +105°C (AEC-Q100 Auto)	353-ball FCCSP (16 x 16 mm)	PCI1004T-V/5CWVAO
PCI1005 7-Port: 1x4UFP 6x2DFP 0 NTBs	Tray	0°C to +70°C (Commercial)	353-ball FCCSP (16 x 16 mm)	PCI1005/5CW
	Tray	-40°C to +85°C (Industrial)	353-ball FCCSP (16 x 16 mm)	PCI1005-I/5CW
	Tape & Reel	0°C to +70°C (Commercial)	353-ball FCCSP (16 x 16 mm)	PCI1005T/5CW
	Tape & Reel	-40°C to +85°C (Industrial)	353-ball FCCSP (16 x 16 mm)	PCI1005T-I/5CW

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